VHDL Keywords

Word	Definition
Abs	Operator, absolute value of right operand. No () Needed.
Access	Used to define an access type, pointer
After	Specifies a time after NOW
Alias	Create another name for an existing identifier
All	Dereferences what precedes the .all
And	Operator, logical “and” of left and right operands
Architecture	A secondary design unit
Array	Used to define an array, vector or matrix
Assert	Used to have a program check on itself

VHDL Keywords

Word	Definition
Attribute	used to declare attribute functions
Begin	start of a begin end pair
Block	start of a block structure
Body	designates a procedure body rather than declaration
Buffer	a mode of a signal, holds a value
Bus	a mode of a signal, can have multiple drivers
Case	part of a case statement
Component	starts the definition of a component
Configuration	a primary design unit

VHDL Keywords

Word	Definition
Constant	declares an identifier to be read only
Disconnect	signal driver condition
Downto	middle of a range 31 downto 0
Else	part of "if" statement, if cond then … else … end if;
Elsif	part of "if" statement, if cond then … elsif cond …
End	part of many statements, may be followed by word and id
Entity	a primary design unit
Exit	sequential statement, used in loops
File	used to declare a file type

VHDL Keywords

Word	Definition
For	start of a for type loop statement
Function	starts declaration and body of a function
Generate	make copies, possibly using a parameter
Generic	introduces generic part of a declaration
Group	collection of types that can get an attribute
Guarded	causes a wait until a signal changes from False to True
If	used in "if" statements
Impure	an impure function is assumed to have side effects
In	indicates a parameter in only input, not changed

VHDL Keywords

Word	Definition
Inertial	signal characteristic, holds a value
Inout	indicates a parameter is used and computed in and out
Is	used as a connective in various statements
Label	used in attribute statement as entity specification
Library	context clause, designates a simple library name
Linkage	a mode for a port, used like **buffer** and **inout**
Literal	used in attribute statement as entity specification
Loop	sequential statement, loop … end loop;
Map	used to map actual parameters, as in port map

VHDL Keywords

Word	Definition
Mod	operator, left operand modulo right operand
Nand	operator, "nand" of left and right operands
New	allocates memory and returns access pointer
Next	sequential statement, used in loops
Nor	operator, "nor" of left and right operands
Not	operator, complement of right operand
Null	sequential statement and a value
Of	used in type declarations, **of** Real ;
On	used as a connective in various statements

VHDL Keywords

Word	Definition
Open	initial file characteristic
Or	operator, logical "or" of left and right operands
Others	fill in missing, possibly all, data
Out	indicates a parameter is computed and output
Package	a design unit, also package body
Port	interface definition, also port map
Postponed	make process wait for all non postponed process to suspend
Procedure	typical programming procedure
Process	sequential or concurrent code to be executed

VHDL Keywords

Word	Definition
Pure	a pure function may not have side effects
Range	used in type definitions, range 1 to 10;
Record	used to define a new record type
Register	signal parameter modifier
Reject	clause in delay mechanism, followed be a time
Rem	operator, remainder of left operand divided by right op
Report	statement and clause in assert statement, string output
Return	statement in procedure or function
Rol	operator, left operand rotated left by right operand

VHDL Keywords

Word	Definition
Ror	operator, left operand rotated right by right operand
Select	used in selected signal assignment statement
Severity	used in assertion and reporting, followed by a severity
Signal	declaration that an object is a signal
Shared	used to declare shared objects
Sla	operator, left operand shifted left arithmetic by right op
Sll	operator, left operand shifted left logical by right op
Sra	operator, left operand shifted right arithmetic by right
Srl	operator, left operand shifted right logical by right op

VHDL Keywords

Word	Definition
Subtype	declaration to restrict an existing type
Then	part of if condition then …
To	middle of a range 1 to 10
Transport	signal characteristic
Type	declaration to create a new type
Unaffected	used in signal waveform
Units	used to define new types of units
Until	used in wait statement
Use	make a package available to this design unit

VHDL Keywords

Word	Definition
Variable	declaration that an object is a variable
Wait	sequential statement, also used in case statement
When	used for choices in case and other statements
While	kind of loop statement
With	used in selected signal assignment statement
Xnor	operator, exclusive "nor" of left and right operands
Xor	perator, exclusive "or" of left and right operands