

Module 7.2

# Quartus II

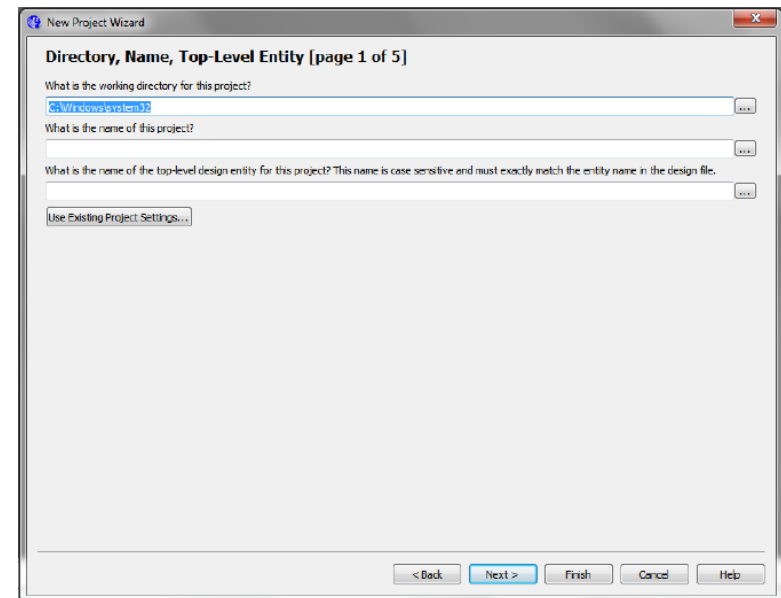
# Quartus II

- Quartus II is used to generate a FPGA programming file
- We cannot use this tool to program the BASYS 2 board



# Create New Project

- Under the “What is the working directory of this project?” dialog box, navigate to the folder where your VHDL code is located
- In the “what is the name of this project” dialog box, enter the name of your VHDL design entity
- Click Next



# Adding Files

- This is where you will add all the VHDL design files.
- Note you will not be adding the test bench, the test bench is for simulation purposes only
- Click Next

# Select your Device

New Project Wizard

## Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family:

Devices:

Target device

Auto device selected by the Fitter

Specific device selected in 'Available devices' list

Other: n/a

Show in 'Available devices' list

Package:

Pin count:

Speed grade:

Name filter:

Show advanced devices  HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	G
EP4CE6E22A7	1.2V	6272	92	276480	30	2	10
EP4CE6E22C6	1.2V	6272	92	276480	30	2	10
EP4CE6E22C7	1.2V	6272	92	276480	30	2	10
EP4CE6E22C8	1.2V	6272	92	276480	30	2	10
EP4CE6E22C8L	1.0V	6272	92	276480	30	2	10
EP4CE6E22C9L	1.0V	6272	92	276480	30	2	10
EP4CF6E2217	1.2V	6272	92	276480	30	2	10

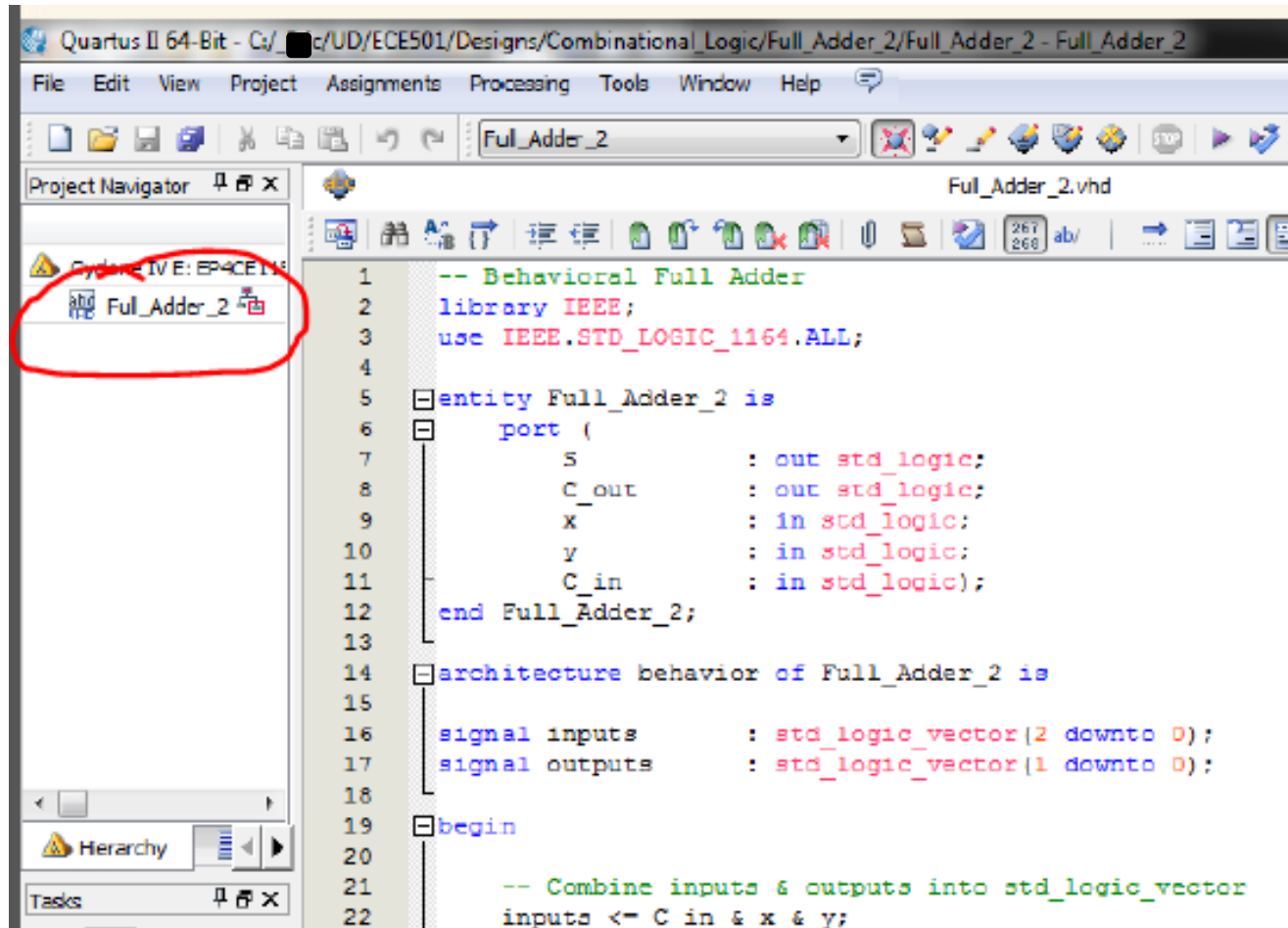
Companion device

HardCopy:

Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

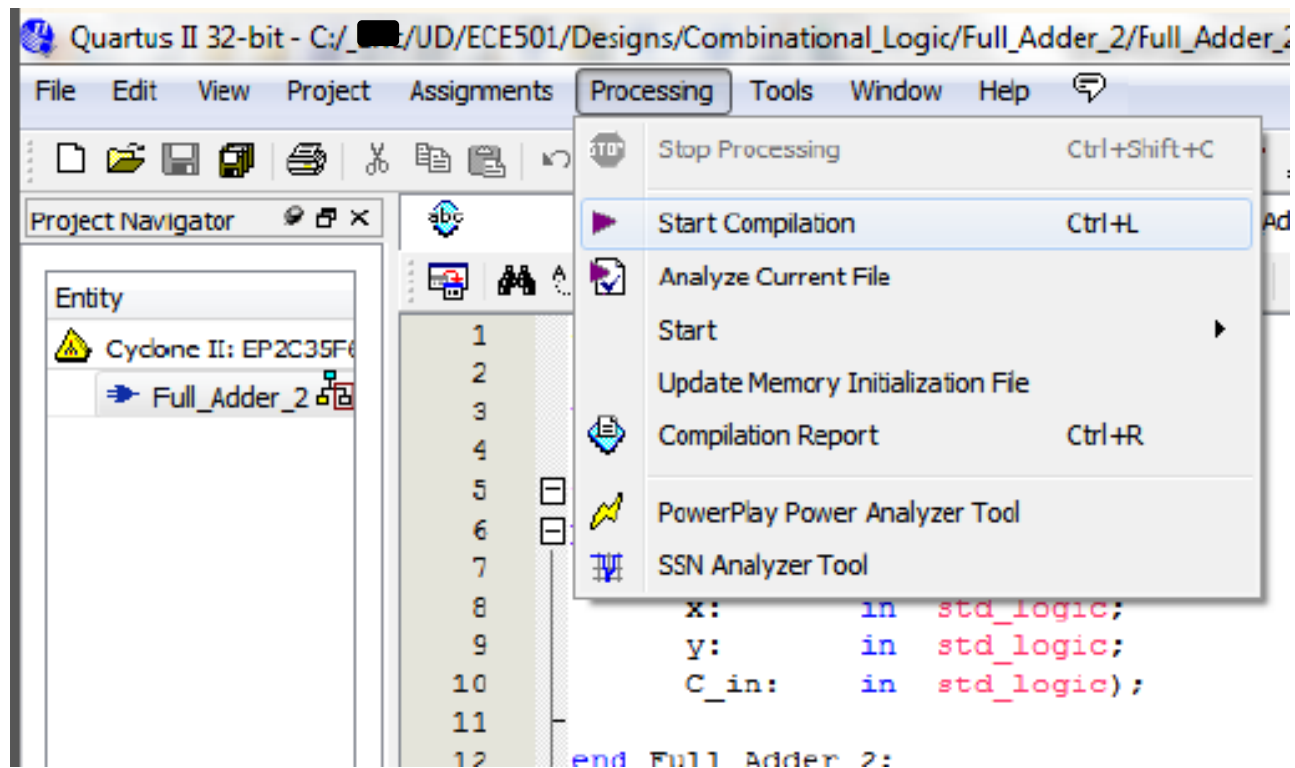
# Project



The screenshot displays the Quartus II 64-bit IDE interface. The title bar indicates the project path: "Quartus II 64-Bit - C:/.../UD/ECE501/Designs/Combinational\_Logic/Full\_Adder\_2/Full\_Adder\_2 - Full\_Adder\_2". The menu bar includes "File", "Edit", "View", "Project", "Assignments", "Processing", "Tools", "Window", and "Help". The toolbar contains various icons for file operations and simulation. The Project Navigator on the left shows a tree view with "Full\_Adder\_2" selected and circled in red. The main editor window displays the VHDL code for "Full\_Adder\_2.vhd".

```
1  -- Behavioral Full Adder
2  library IEEE;
3  use IEEE.STD_LOGIC_1164.ALL;
4
5  entity Full_Adder_2 is
6  port (
7      S           : out std_logic;
8      C_out       : out std_logic;
9      x           : in  std_logic;
10     y           : in  std_logic;
11     C_in        : in  std_logic);
12  end Full_Adder_2;
13
14  architecture behavior of Full_Adder_2 is
15
16     signal inputs      : std_logic_vector(2 downto 0);
17     signal outputs     : std_logic_vector(1 downto 0);
18
19  begin
20
21     -- Combine inputs & outputs into std_logic_vector
22     inputs <= C_in & x & y;
```

# Compilation



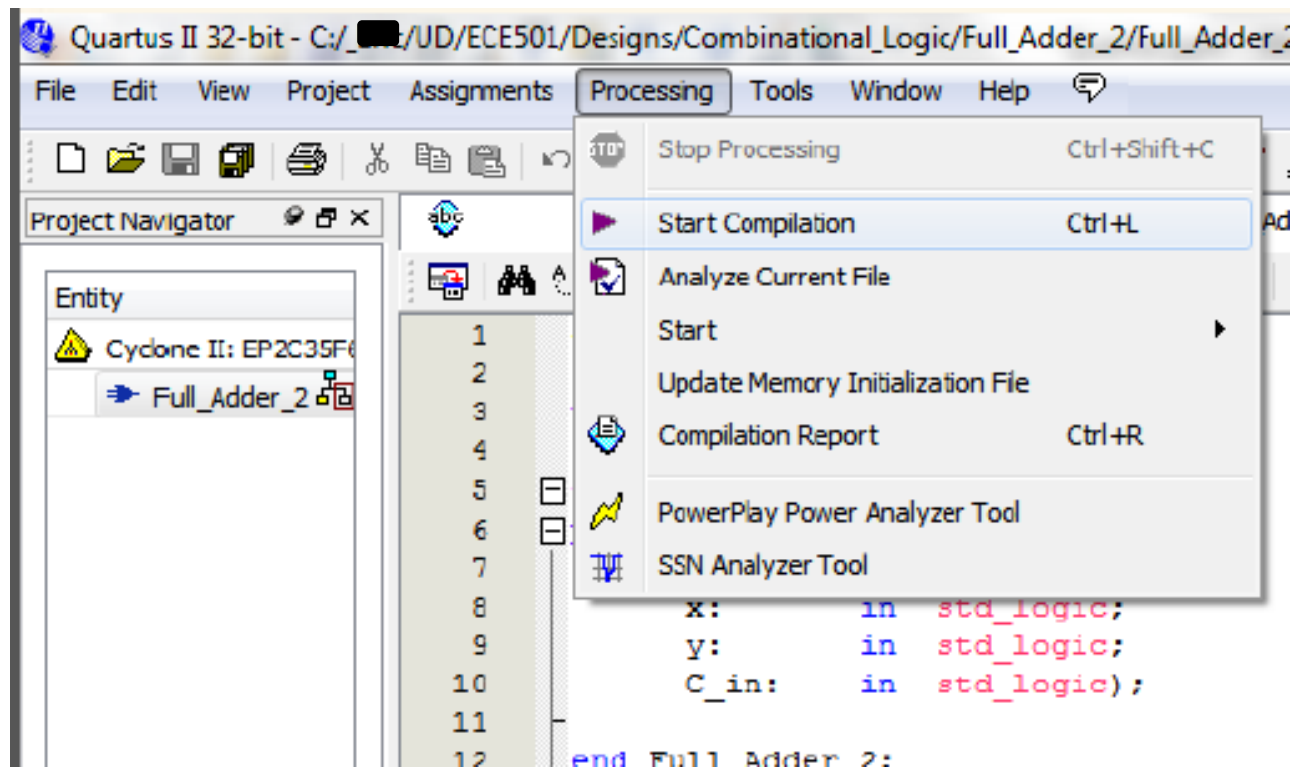
# I/O Routing

The screenshot displays the Quartus II 32-bit software interface. The main window title is "Quartus II 32-bit - C:/.../UD/ECE501/Designs/Combinational\_Logic/Full\_Adder\_2/Full\_Adder\_2 - Full\_Adder\_2". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The Assignments menu is open, showing options such as Device..., Settings..., TimeQuest Timing Analyzer Wizard..., Assignment Editor, Pin Planner, Remove Assignments..., Back-Annotate Assignments..., Import Assignments..., Export Assignments..., Assignment Groups..., LogicLock Regions Window, and Design Partitions Window. The Pin Planner option is highlighted. The Project Navigator on the left shows the entity hierarchy for "Cyclone II: EP2C35F672C6" and "Full\_Adder\_2". The bottom right corner of the window shows a summary table of resource usage.

Total memory bits	0 / 483,840 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 70 ( 0 % )
Total PLLs	0 / 4 ( 0 % )



# Re - Compilation



# Program Device

The screenshot shows the Quartus II 64-bit software interface. The title bar reads "Quartus II 64-Bit - C:/.../UD/ECE501/Designs/Combinational\_Logic/Full\_Adder\_2/Full\_Adder\_2 - Full\_Adder\_2". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The "Tools" menu is open, listing various utilities such as "Run Simulation Tool", "Launch Simulation Library Compiler", "Launch Design Space Explorer", "TimeQuest Timing Analyzer", "Advisors", "Chip Planner", "Design Partition Planner", "Netlist Viewers", "SignalTap II Logic Analyzer", "In-System Memory Content Editor", "Logic Analyzer Interface Editor", "In-System Sources and Probes Editor", "SignalProbe Pins...", "Programmer", "JTAG Chain Debugger", "System Console", "MegaWizard Plug-In Manager", "Nios II Software Build Tools for Eclipse", "Qsys", and "Td Scripts...". The "Programmer" option is highlighted. In the background, the Project Navigator shows "Cyclone IV E: EP4CE115F29C7" and "Full\_Adder\_2". The Tasks pane at the bottom shows a list of tasks including "Compile Design", "Analysis & Synthesis", "Edit Settings", "View Report", "Analysis & Elaboration", and "Partition Merge".

The screenshot shows the Quartus II Programmer window. The title bar reads "Programmer - C:/.../UD/ECE501/Designs/Combinational\_Logic/Full\_Adder\_2/Full\_...". The menu bar includes File, Edit, View, Processing, Tools, Window, and Help. The "Hardware Setup..." button is active, showing "No Hardware" and "Mode: JTAG". A checkbox for "Enable real-time ISP to allow background programming (for MAX II and MAX V devices)" is checked. Below the hardware setup are buttons for "Start", "Stop", "Auto Detect", "Delete", "Add File...", "Change File...", "Save File", and "Add Device...". A table displays the current configuration:

File	Device	Checksum
output_files/Full_Adder_2...	EP4CE115F29	00563438

At the bottom, a diagram shows a device labeled "ADDERA EP4CE115F29" with a "TDI" input and a "TDO" output.

# Summary

- Use this module as a reference if you have an Altera board you are wanting to program it
- All of the designs utilized in the labs will work and run on an Altera development board