Module 7.2

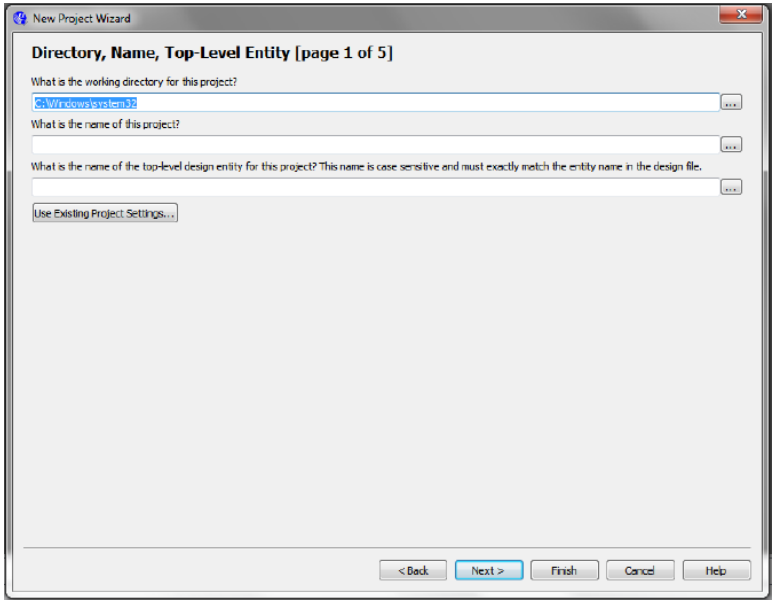
Quartus II

Quartus II

- Quartus II is used to generate a FPGA programming file
- We cannot use this tool to program the BASYS 2 board

Create New Project

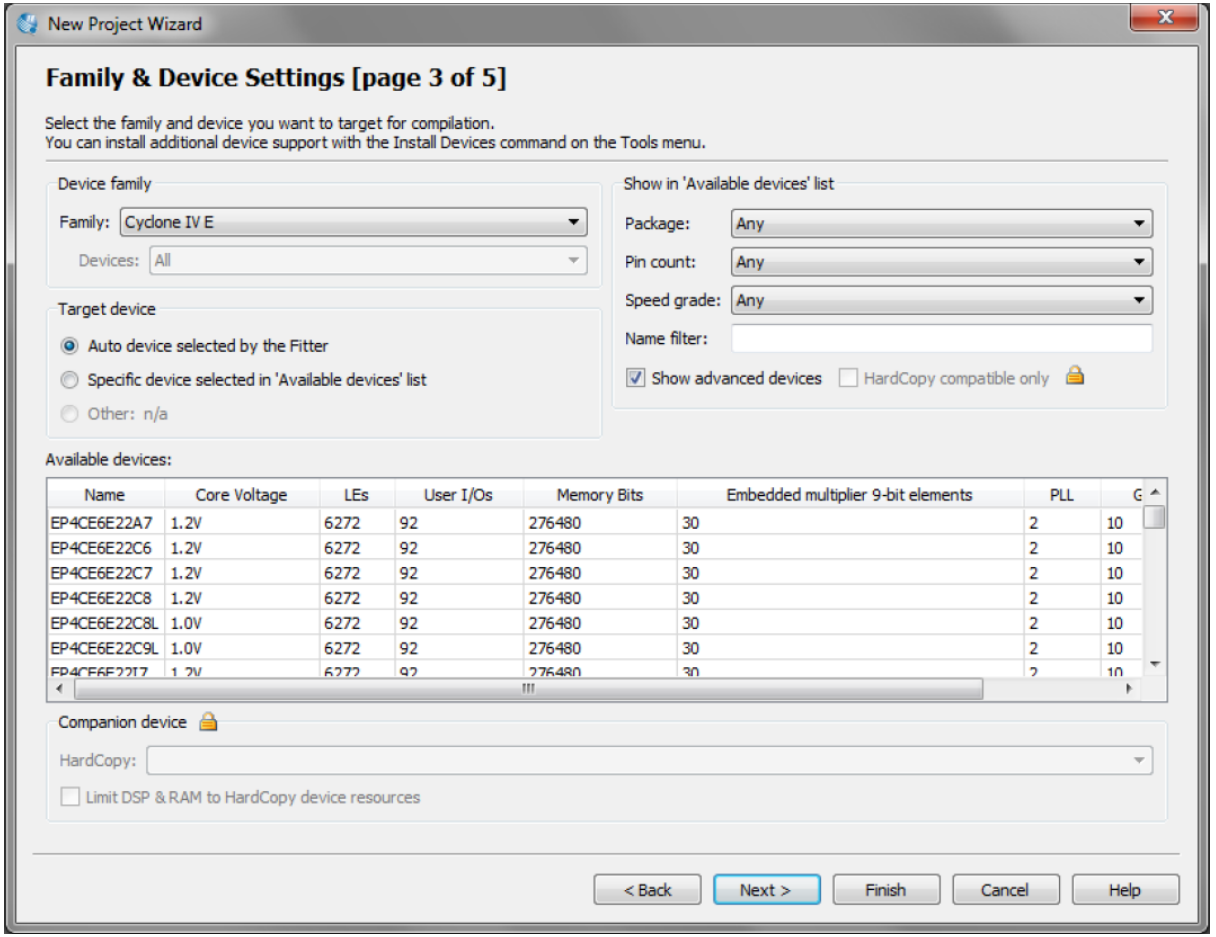
- Under the "What is the working directory of this project?" dialog box, navigate to the folder where your VHDL code is located
- In the "what is the name of this project" dialog box, enter the name of your VHDL design entity
- Click Next



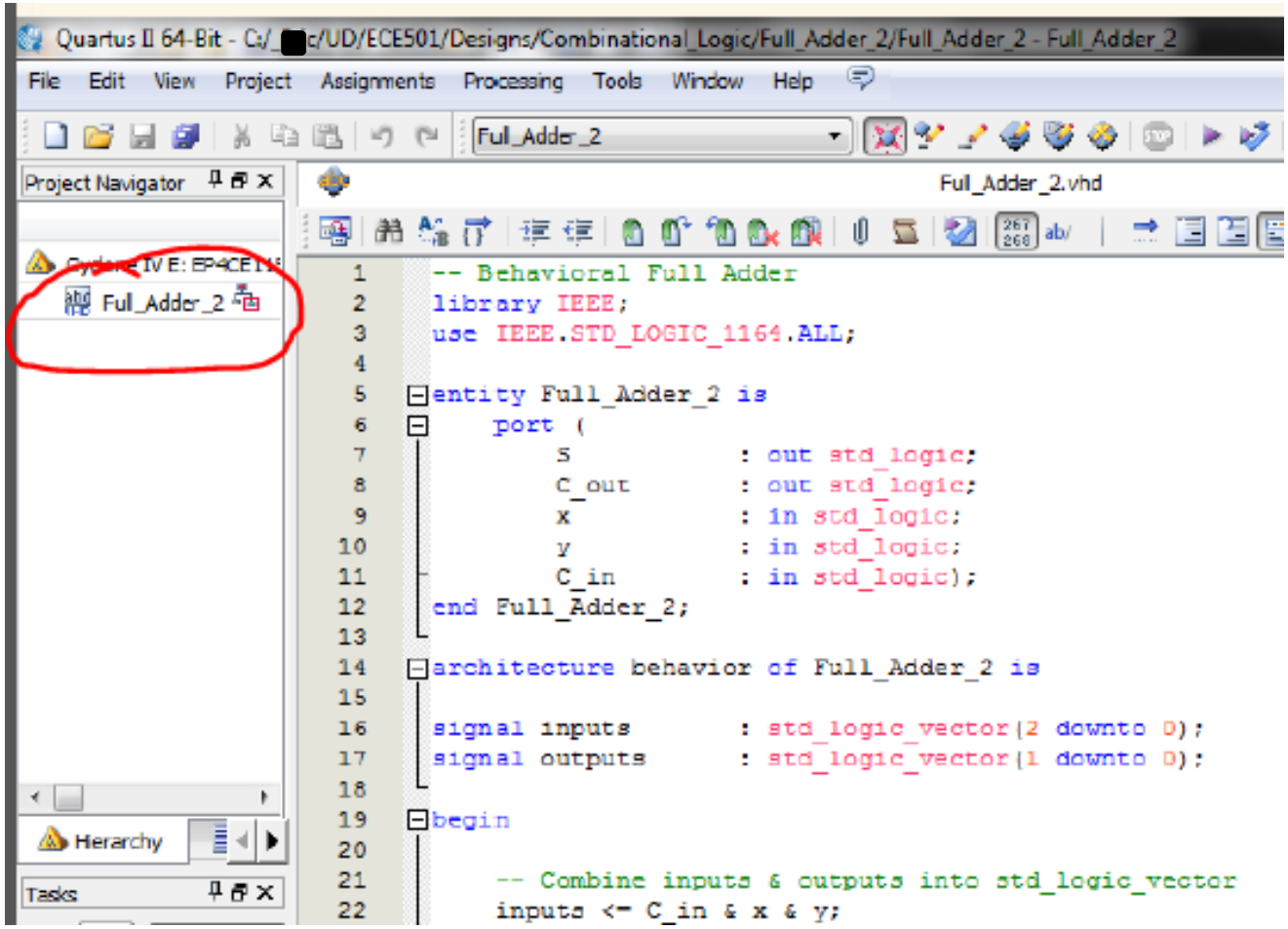
Adding Files

- This is where you will add all the VHDL design files.
- Note you will not be adding the test bench, the test bench is for simulation purposes only
- Click Next

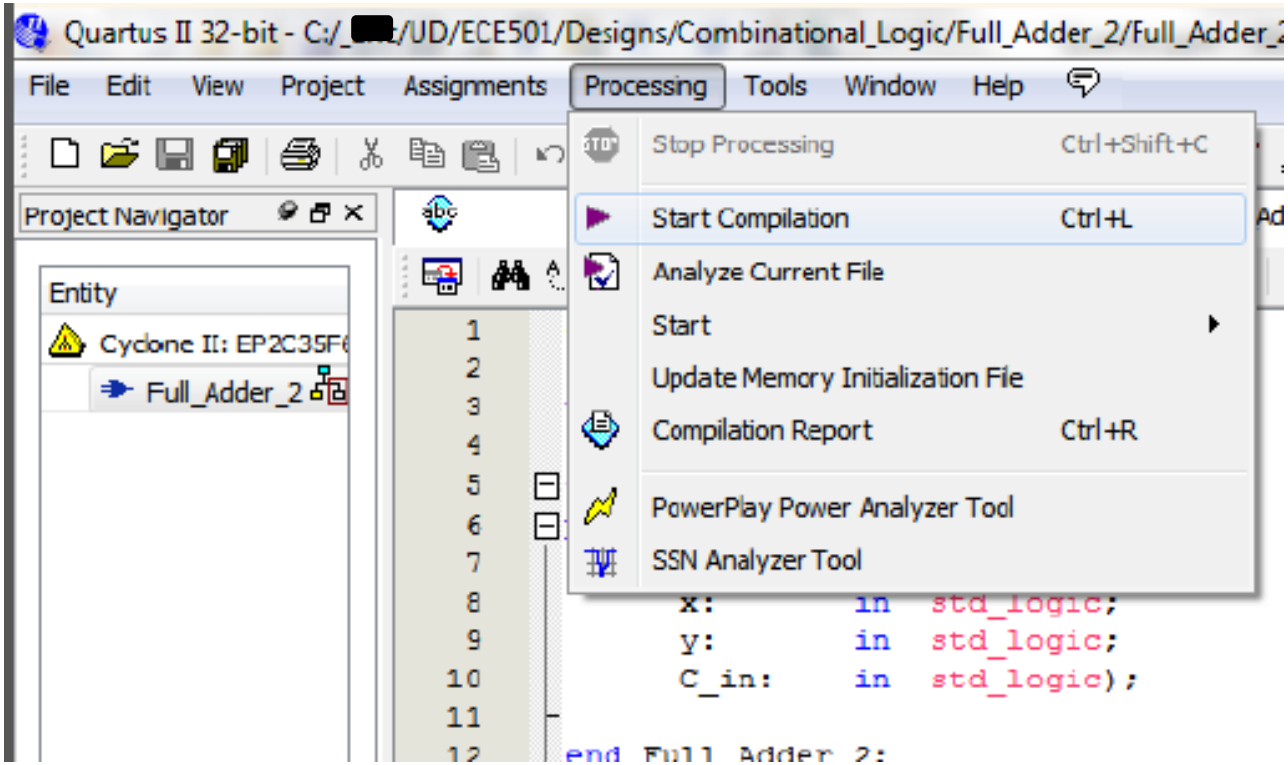
Select your Device



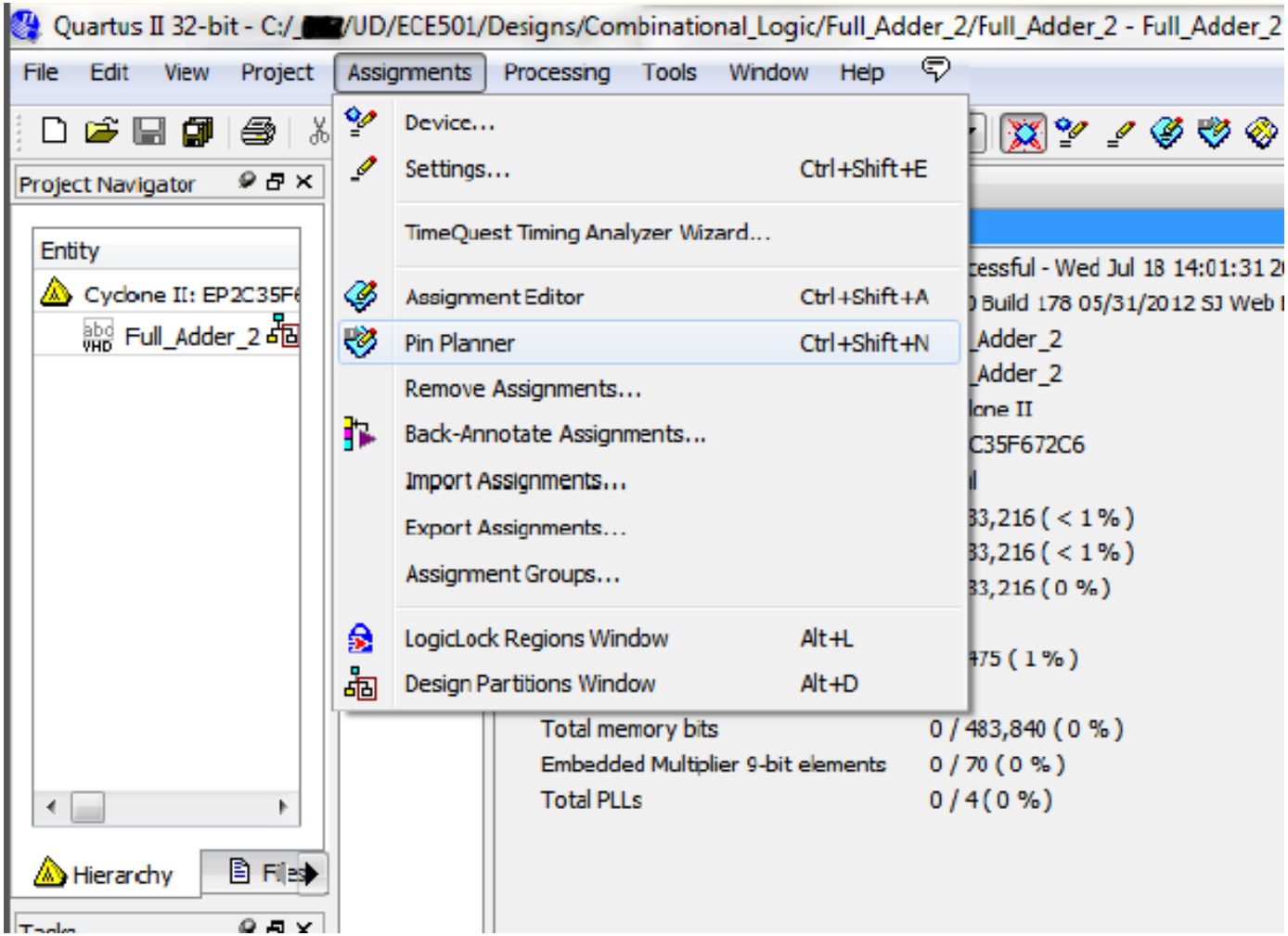
Project


Quartus II 64-Bit - C:/[redacted]c/UD/ECE501/Designs/Combinational_Logic/Full_Adder_2/Full_Adder_2 - Full_Adder_2
File Edit View Project Assignments Processing Tools Window Help
Full_Adder_2
Project Navigator
Full_Adder_2.vhd
Full_Adder_2
Hierarchy
Tasks
1 -- Behavioral Full Adder
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4
5 entity Full_Adder_2 is
6 port (
7 S : out std_logic;
8 C_out : out std_logic;
9 x : in std_logic;
10 y : in std_logic;
11 C_in : in std_logic);
12 end Full_Adder_2;
13
14 architecture behavior of Full_Adder_2 is
15
16 signal inputs : std_logic_vector(2 downto 0);
17 signal outputs : std_logic_vector(1 downto 0);
18
19 begin
20
21 -- Combine inputs & outputs into std_logic_vector
22 inputs <= C_in & x & y;

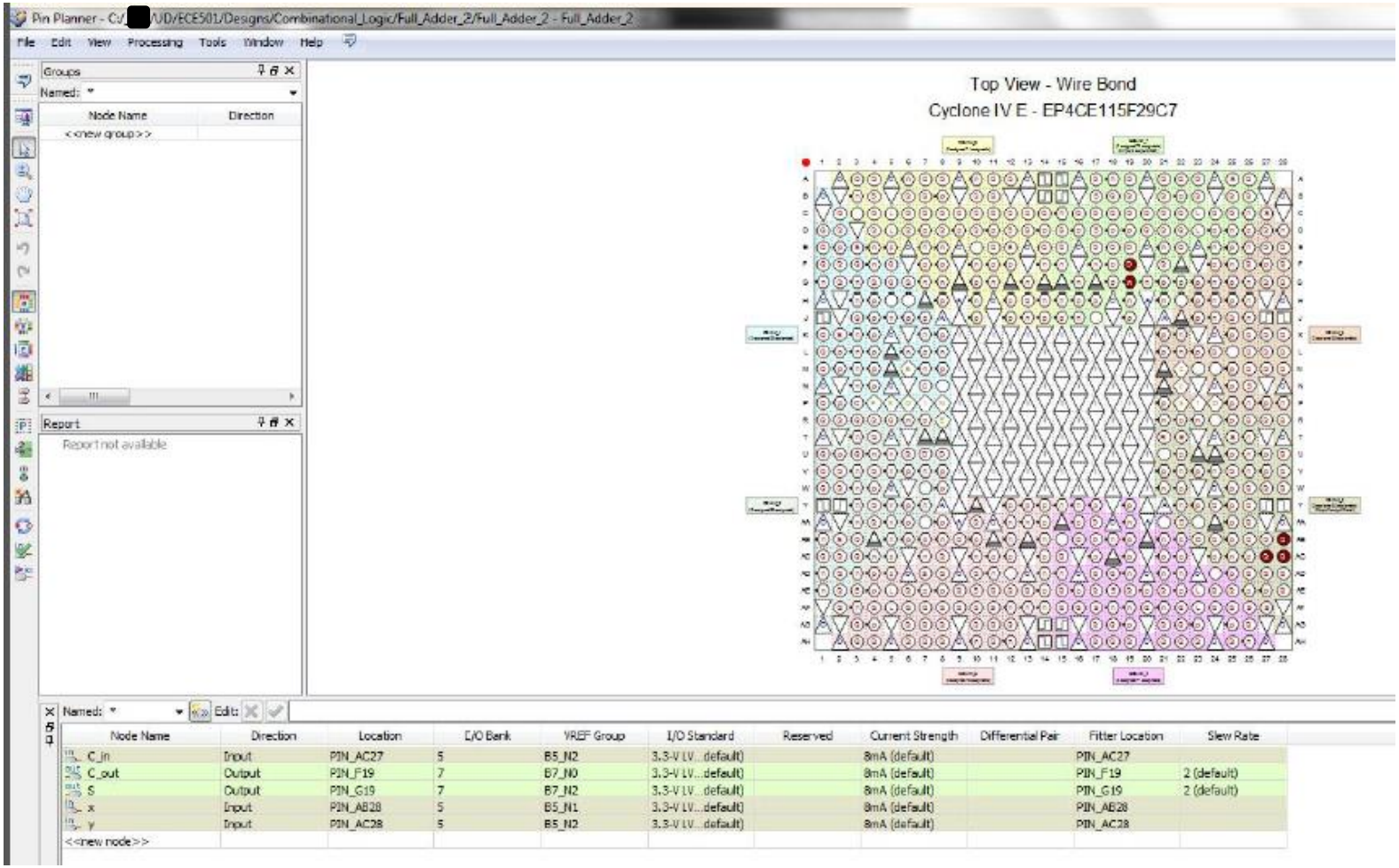
Compilation



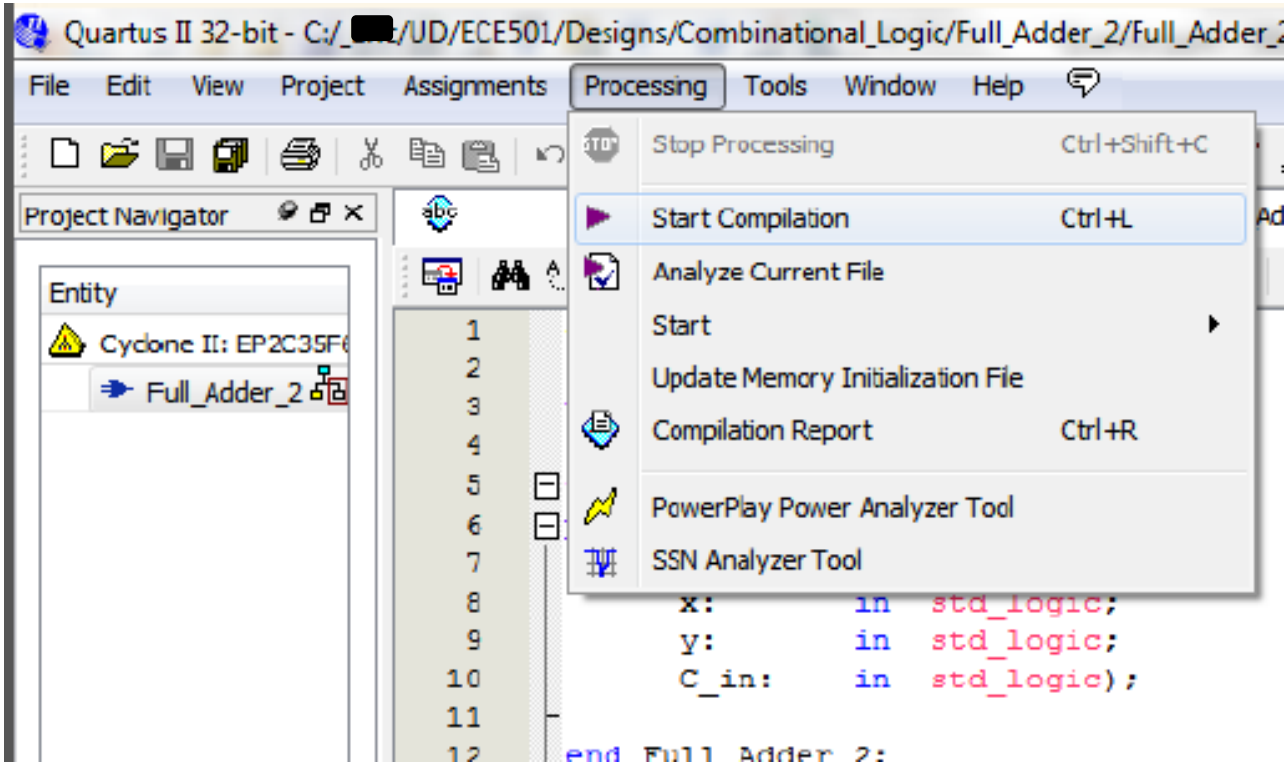
I/O Routing


Quartus II 32-bit - C:/[redacted]/UD/ECE501/Designs/Combinational_Logic/Full_Adder_2/Full_Adder_2 - Full_Adder_2
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Project Navigator
Entity
Cyclone II: EP2C35F6
Full_Adder_2
Hierarchy
Files
Device...
Settings... Ctrl+Shift+E
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D
Total memory bits 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements 0 / 70 (0 %)
Total PLLs 0 / 4 (0 %)

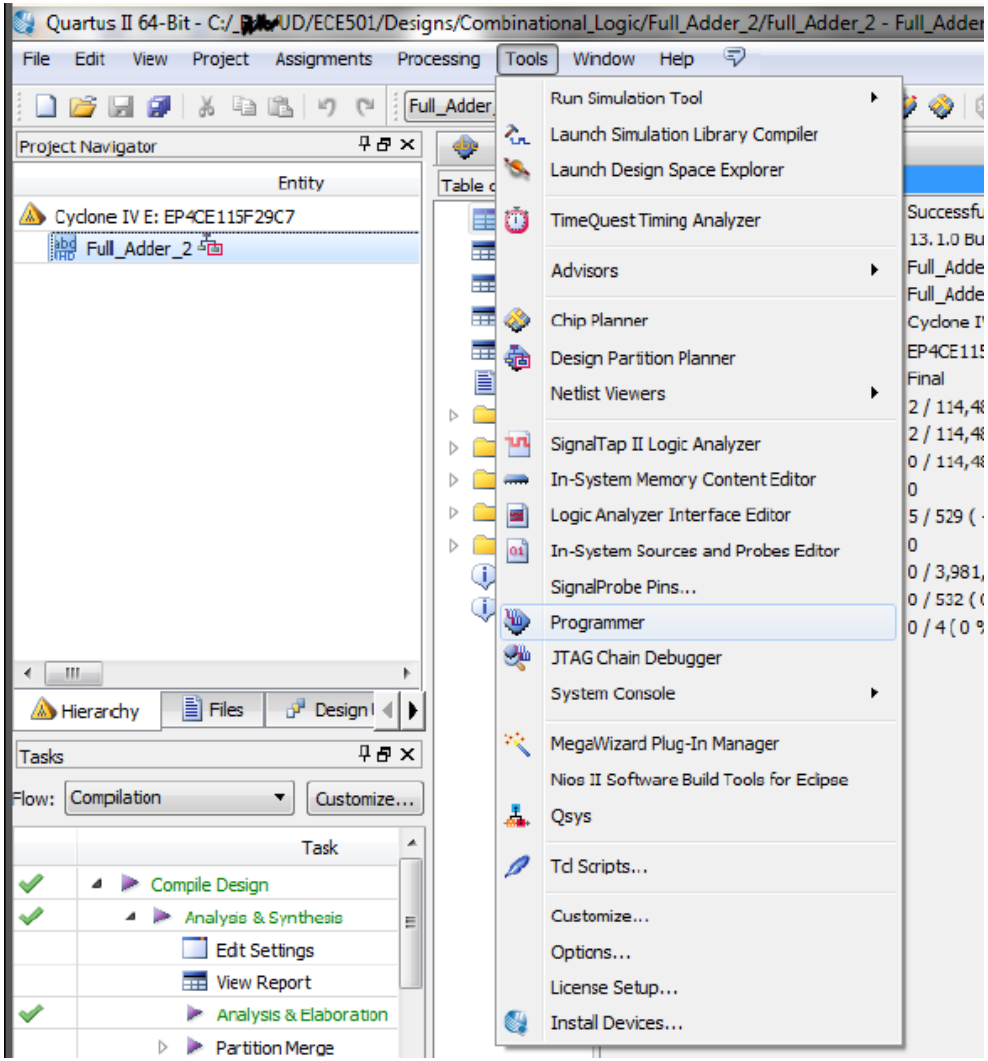
I/O Routing

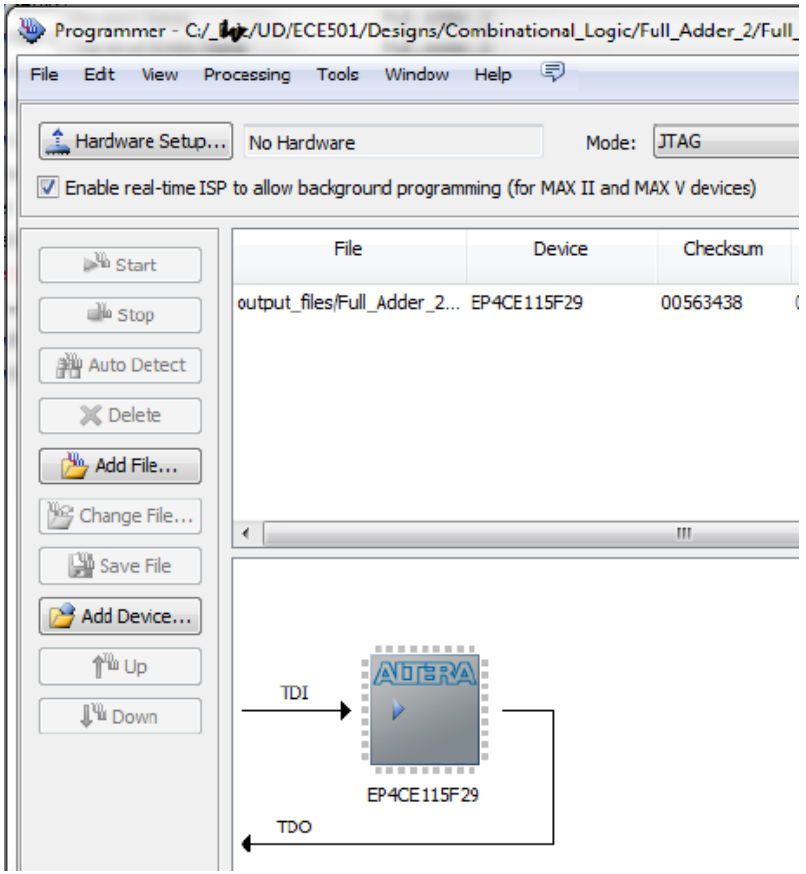

Pin Planner - C:/[redacted]/ECE501/Designs/Combinational_Logic/Full_Adder_2/Full_Adder_2 - Full_Adder_2
File Edit View Processing Tools Window Help
Groups
Named: *
Node Name Direction
<<new group>>
Report
Report not available
Top View - Wire Bond
Cyclone IV E - EP4CE115F29C7
Named: * Edit:
Node Name | Direction | Location | I/O Bank | VREF Group | I/O Standard | Reserved | Current Strength | Differential Pair | Fitter Location | Slew Rate
C_in | Input | PIN_AC27 | 5 | B5_N2 | 3.3-V LV...default) | | 8mA (default) | | PIN_AC27 |
C_out | Output | PIN_F19 | 7 | B7_N0 | 3.3-V LV...default) | | 8mA (default) | | PIN_F19 | 2 (default)
S | Output | PIN_G19 | 7 | B7_N2 | 3.3-V LV...default) | | 8mA (default) | | PIN_G19 | 2 (default)
x | Input | PIN_AB28 | 5 | B5_N1 | 3.3-V LV...default) | | 8mA (default) | | PIN_AB28 |
y | Input | PIN_AC28 | 5 | B5_N2 | 3.3-V LV...default) | | 8mA (default) | | PIN_AC28 |
<<new node>>

Re - Compilation



Program Device





Summary

- Use this module as a reference if you have an Altera board you are wanting to program it
- All of the designs utilized in the labs will work and run on an Altera development board