Module 7.1

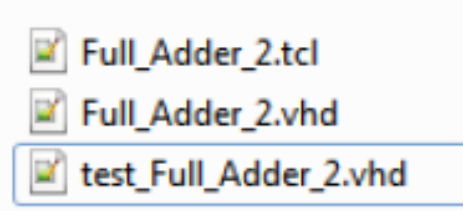
ModelSim

ModelSim

- Used to simulate and test your VHDL design
- Very useful tool for debugging and making sure your design is working properly
- You can test your designs in ModelSim and then synthesize them in Xilinx tool set

Simulation Steps

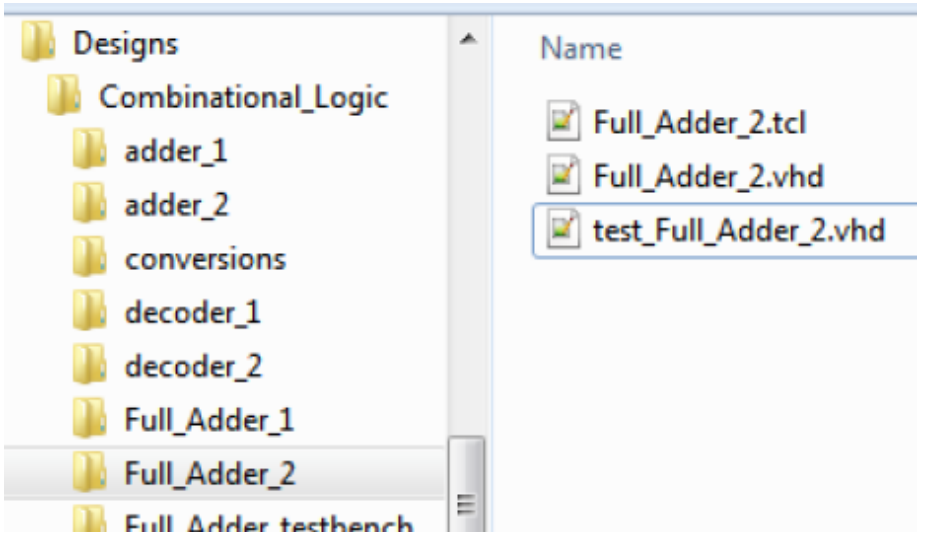
- 1) Code all necessary VHDL files
  - Files include:
    - *.tcl file
    - Design File
    - Test Bench



- 2) Navigate to your VHDL design directory
- 3) Create a ModelSim library
- 4) Compile
- 5) Simulate

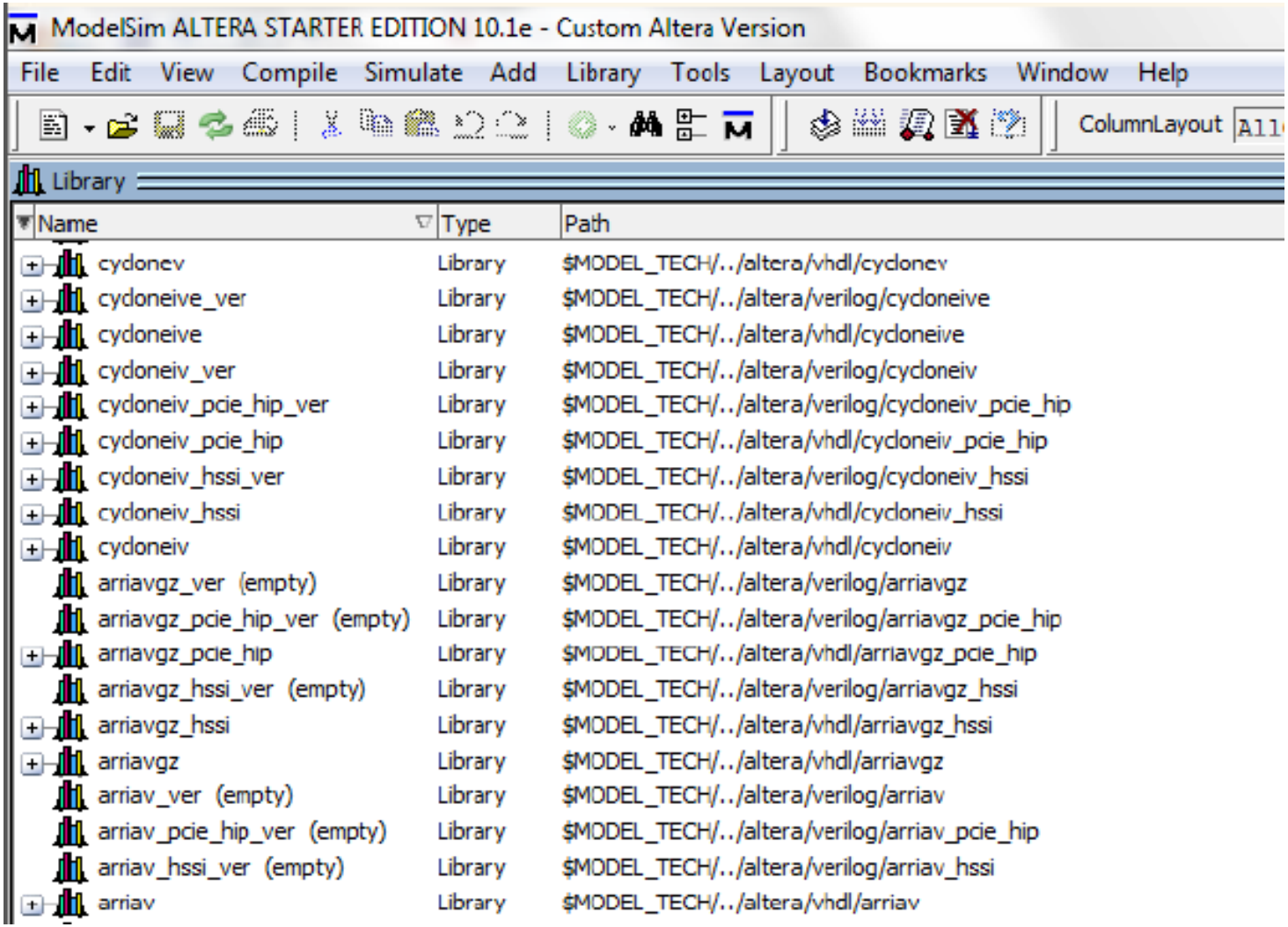
Step 1 Code VHDL files

- Step 1 is to create the necessary VHDL files which include
  - Design file
  - Test Bench
  - A *.tcl file

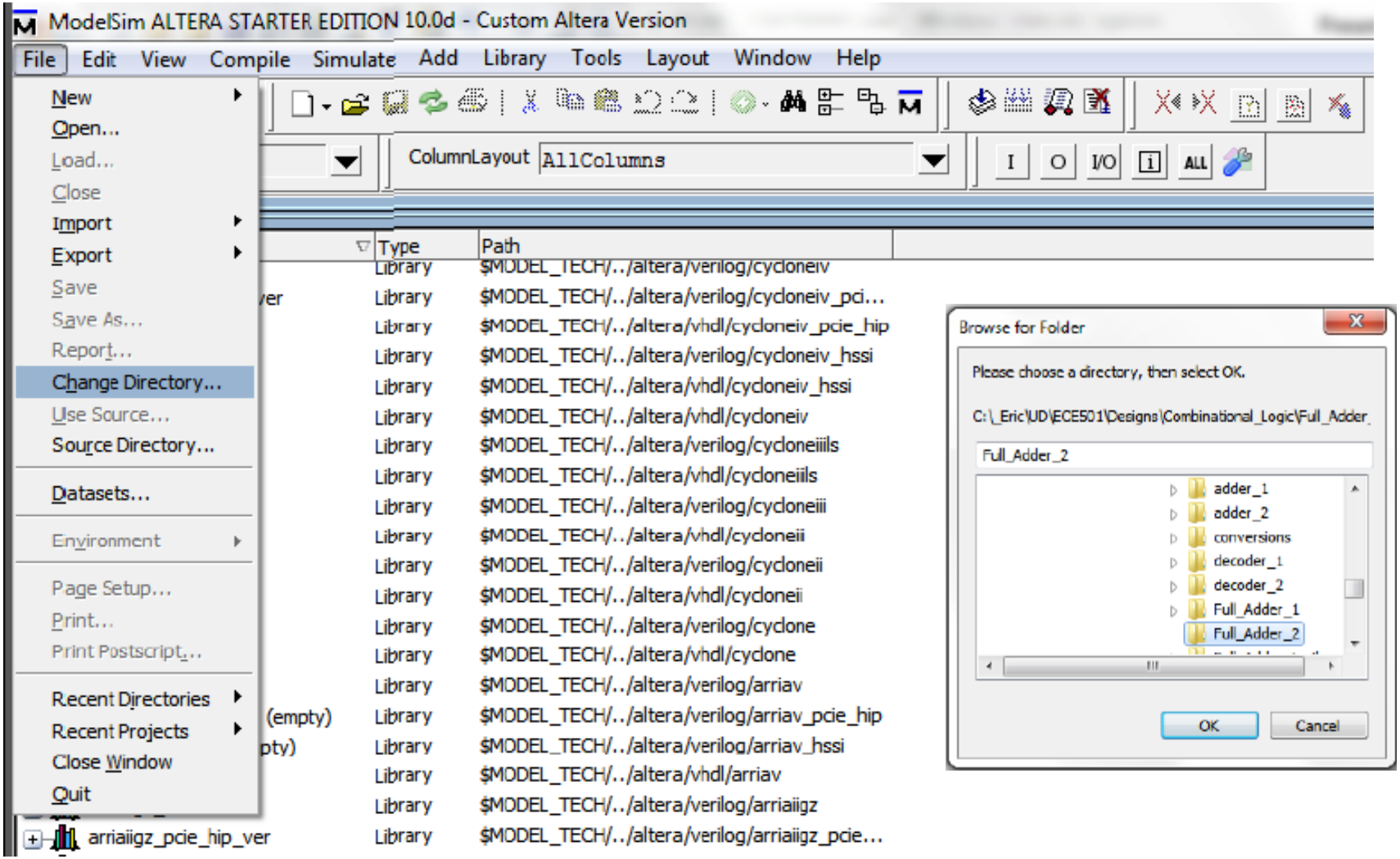


Note the organization this will help when you are looking for a specific design file

Open ModelSim



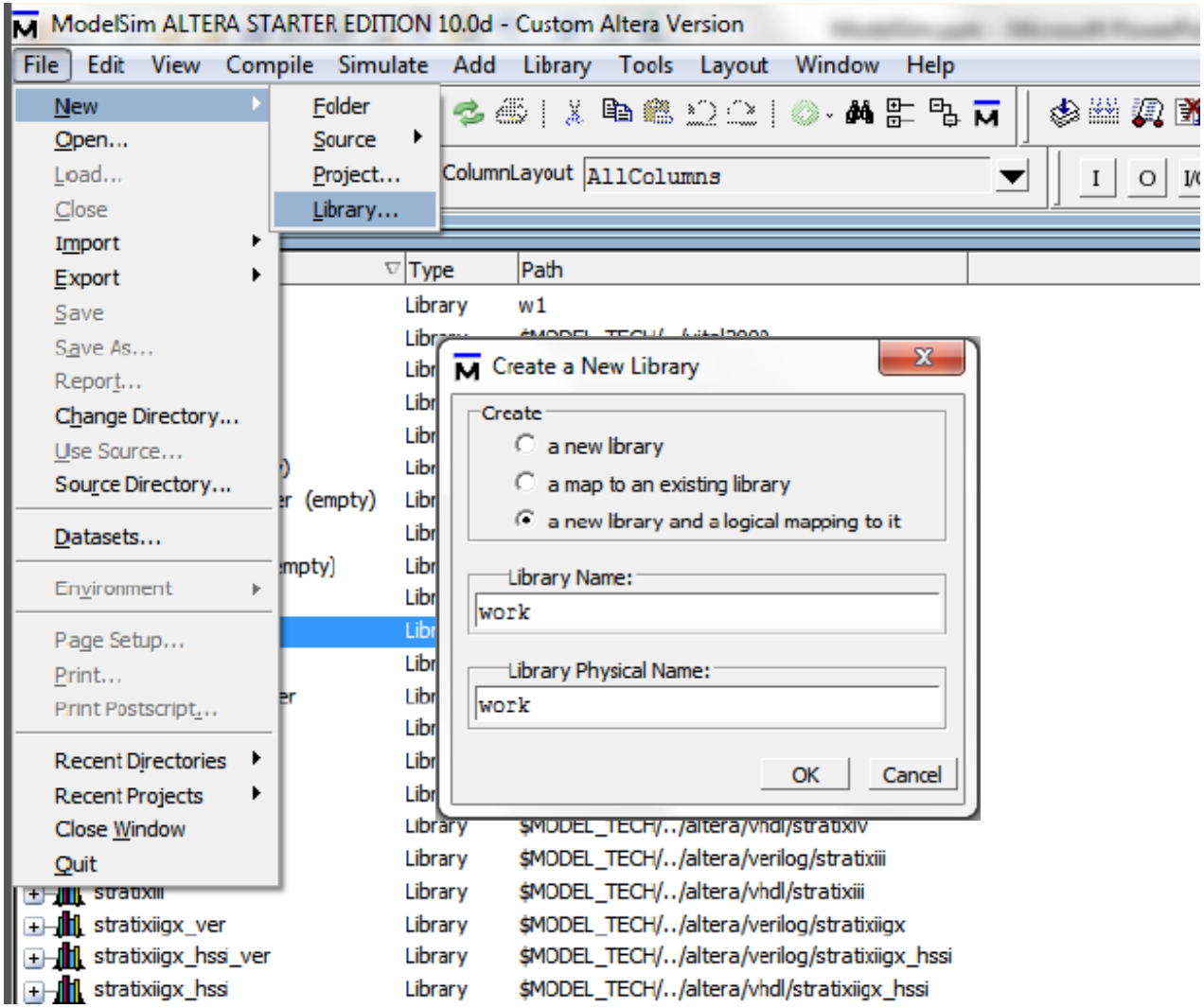
Step 2 Change Directory



Step 3 Create a Library

- For every ModelSim project you create, you need to have a ModelSim library.
- Once you create a library in a directory ModelSim will detect it the next time you navigate to that directory

Step 3 Create a Library



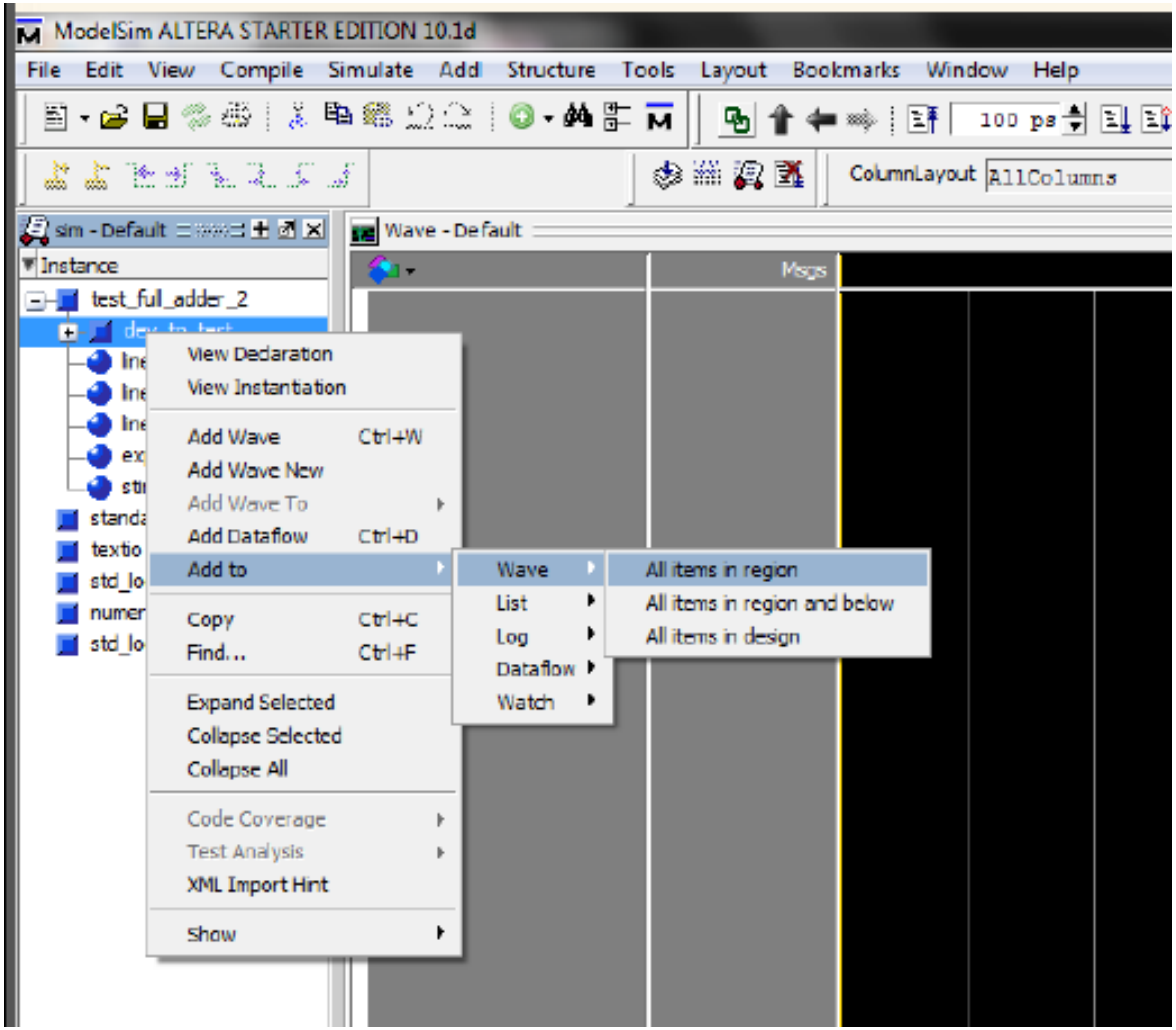
Step 4 Compile

- Select Compile → Compile and then select your VHDL design and the test bench
- Hit Compile
- Both the test bench and design files are VHDL files (extension *.vhd)
- Any errors in your VHDL design or test bench will show up in the transcript window
- If you have any errors, modify the VHDL files and then repeat this process until there are no errors

Step 5 Simulate

- Expand the work library in the library window
- Double click on the test bench VHDL entity
  - This should launch the ModelSim Simulation Window
- In the sim-default window right click on the "dev_to_test" or "UUT" instance and navigate to "add-to wave-all items in region
- Then type "run 80 ns" in the transcript window or however long you want your simulation to run for

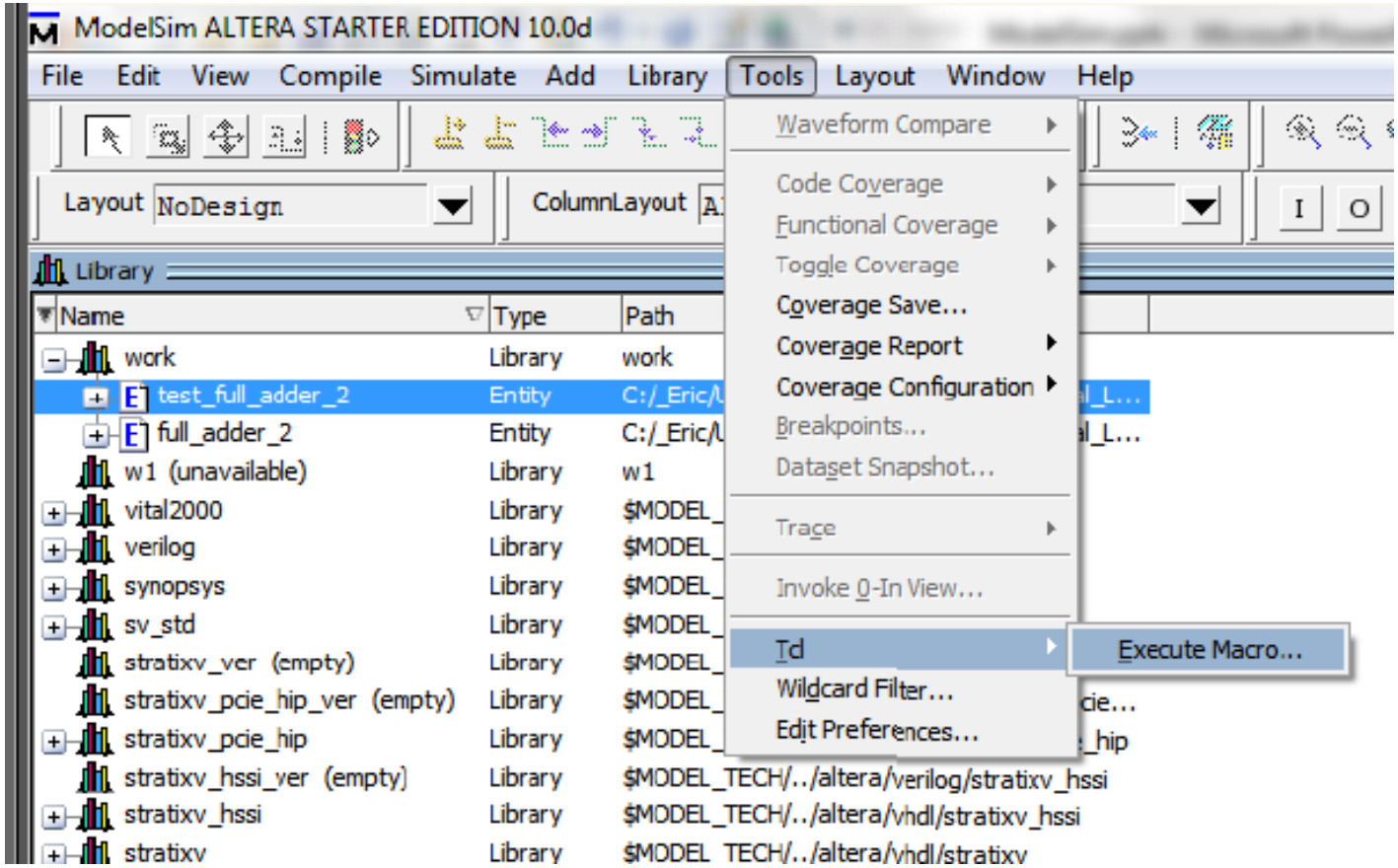
Step 5 Simulate



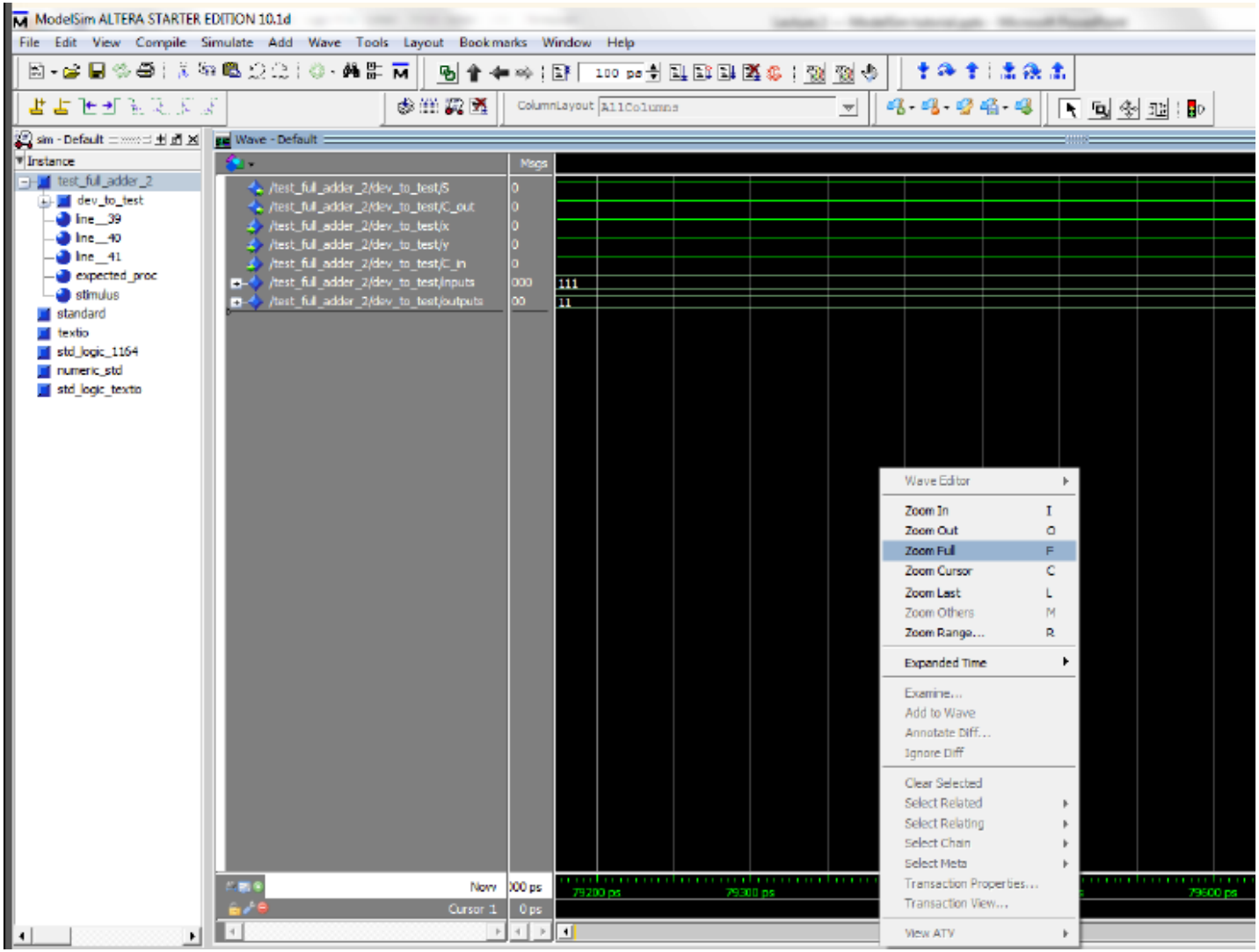
Step 4 & 5

- We can combine steps 4 and 5 in one step with the use of a *.tcl file
- After step 3 click
  - Tools→Tcl→Execute Macro
- This should then select both your VHDL designs compile them and then run the simulation
- I will provide the *.tcl script for all the VHDL designs in the labs

Step 4 & 5

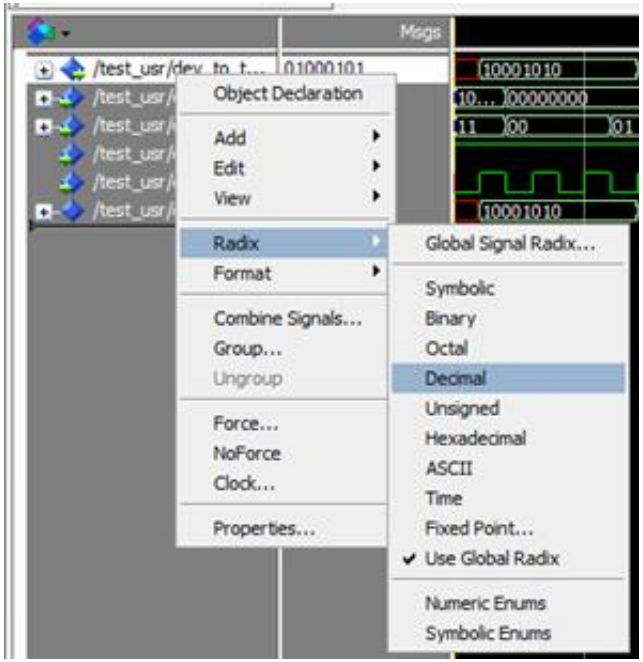

ModelSim ALTERA STARTER EDITION 10.0d
File Edit View Compile Simulate Add Library Tools Layout Window Help
Waveform Compare
Code Coverage
Functional Coverage
Toggle Coverage
Coverage Save...
Coverage Report
Coverage Configuration
Breakpoints...
Dataset Snapshot...
Trace
Invoke 0-In View...
Tcl
Wildcard Filter...
Edit Preferences...
Execute Macro...
Layout NoDesign
ColumnLayout
Library
Name Type Path
work Library work
test_full_adder_2 Entity C:/_Eric/
full_adder_2 Entity C:/_Eric/
w1 (unavailable) Library w1
vital2000 Library $MODEL_
verilog Library $MODEL_
synopsys Library $MODEL_
sv_std Library $MODEL_
stratixv_ver (empty) Library $MODEL_
stratixv_pcie_hip_ver (empty) Library $MODEL_
stratixv_pcie_hip Library $MODEL_
stratixv_hssi_ver (empty) Library $MODEL_TECH/../altera/verilog/stratixv_hssi
stratixv_hssi Library $MODEL_TECH/../altera/vhdl/stratixv_hssi
stratixv Library $MODEL_TECH/../altera/vhdl/stratixv

Tips & Tricks


ModelSim ALTERA STARTER EDITION 10.1d
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
test_full_adder_2
dev_to_test
line__39
line__40
line__41
expected_proc
stimulus
standard
textio
std_logic_1164
numeric_std
std_logic_textio
Wave - Default
Msgs
/test_full_adder_2/dev_to_test/S
/test_full_adder_2/dev_to_test/C_out
/test_full_adder_2/dev_to_test/x
/test_full_adder_2/dev_to_test/y
/test_full_adder_2/dev_to_test/C_in
/test_full_adder_2/dev_to_test/inputs
/test_full_adder_2/dev_to_test/outputs
111
11
Now
Cursor 1
79200 ps
79300 ps
79600 ps
Wave Editor
Zoom In I
Zoom Out O
Zoom Full F
Zoom Cursor C
Zoom Last L
Zoom Others M
Zoom Range... R
Expanded Time
Examine...
Add to Wave
Annotate Diff...
Ignore Diff
Clear Selected
Select Related
Select Relating
Select Chain
Select Meta
Transaction Properties...
Transaction View...
View ATV

Tips & Tricks

- Right click on a signal in the simulation window and select radix and change to the value that makes the most sense



Summary

- You need to have a ModelSim library for every project
- You can manually compile and simulate your designs however using *.tcl scripts are a much easier and faster way of simulating