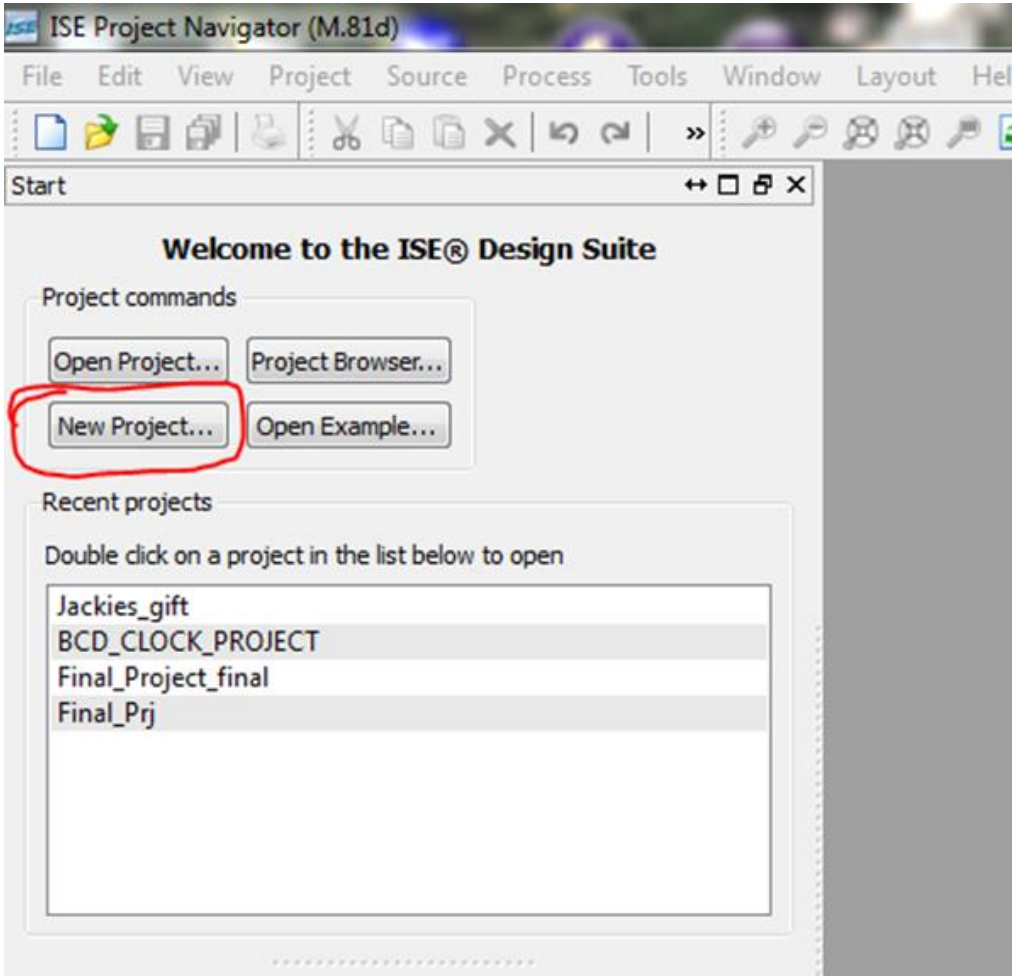
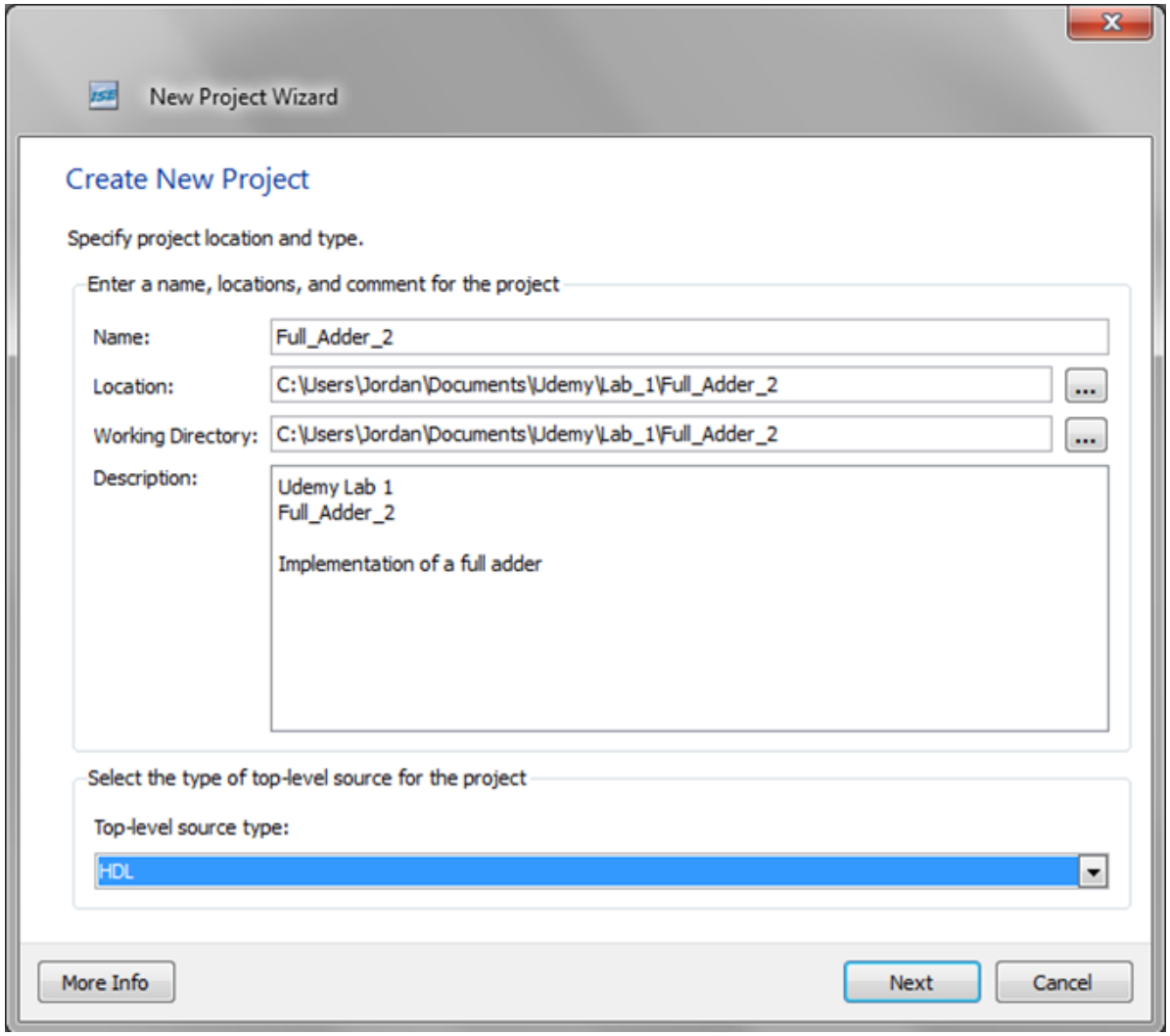
Module 8.2

Xilinx ISE Project

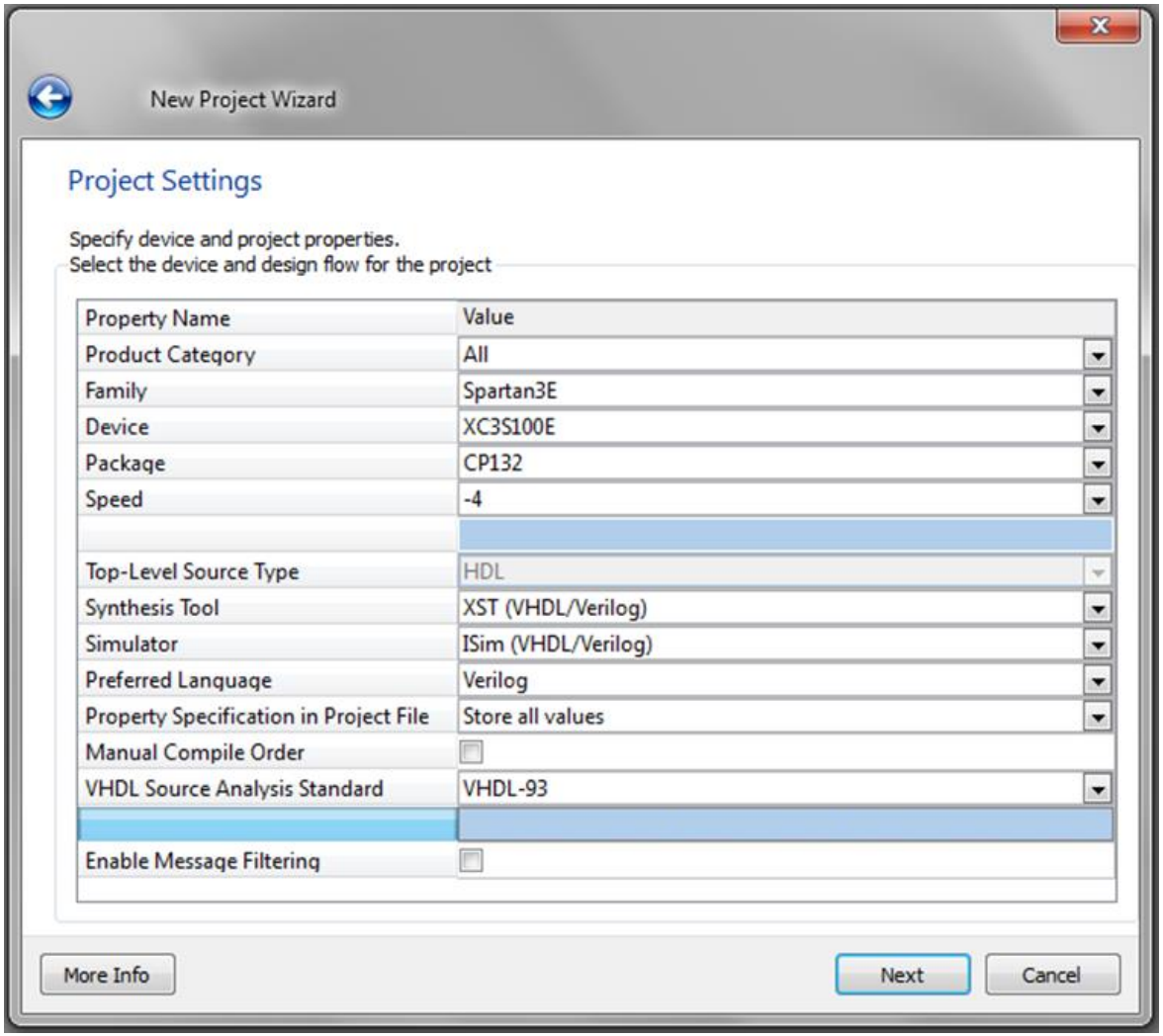
Creating a Project



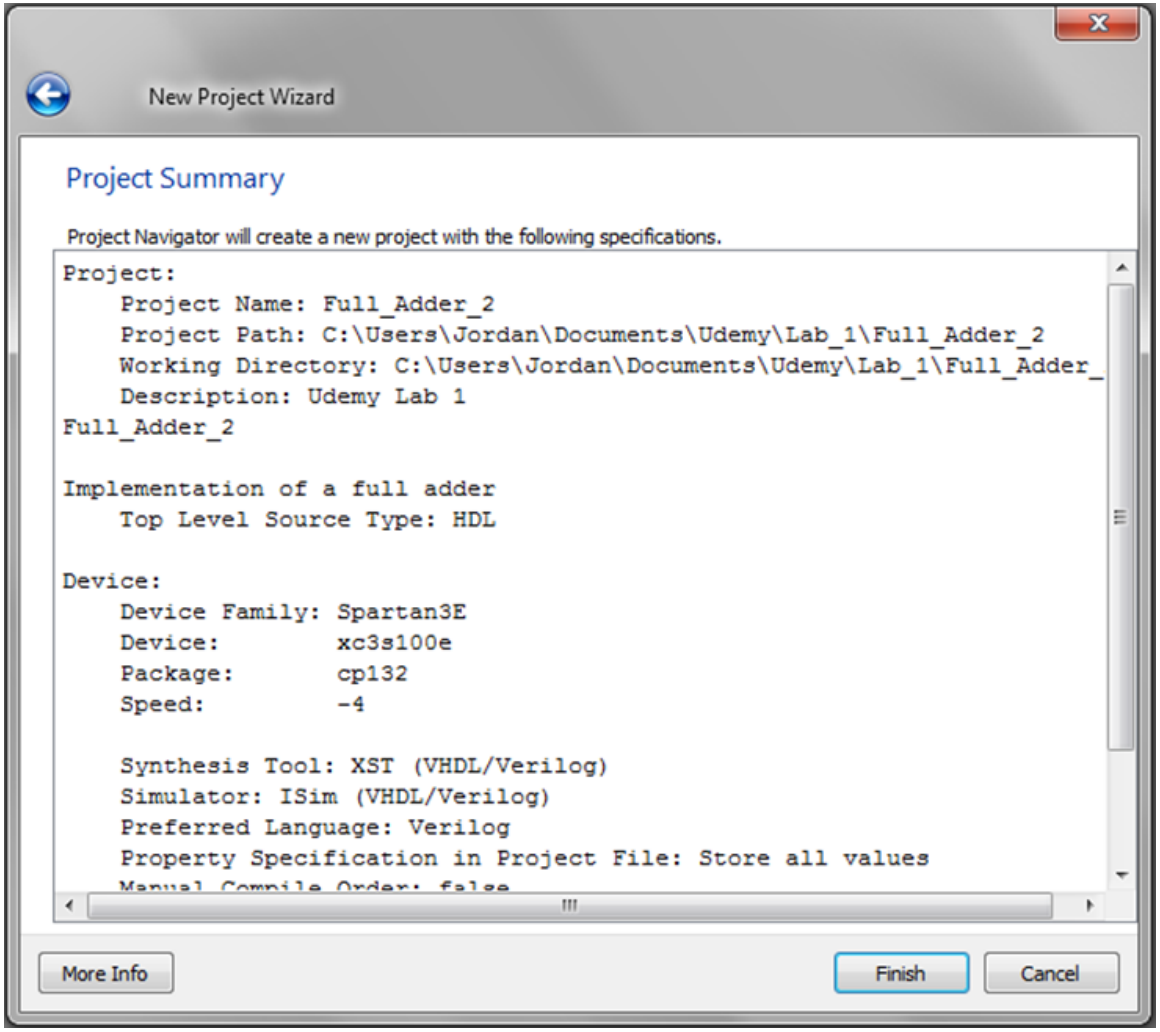
New Project Wizard



Project Settings

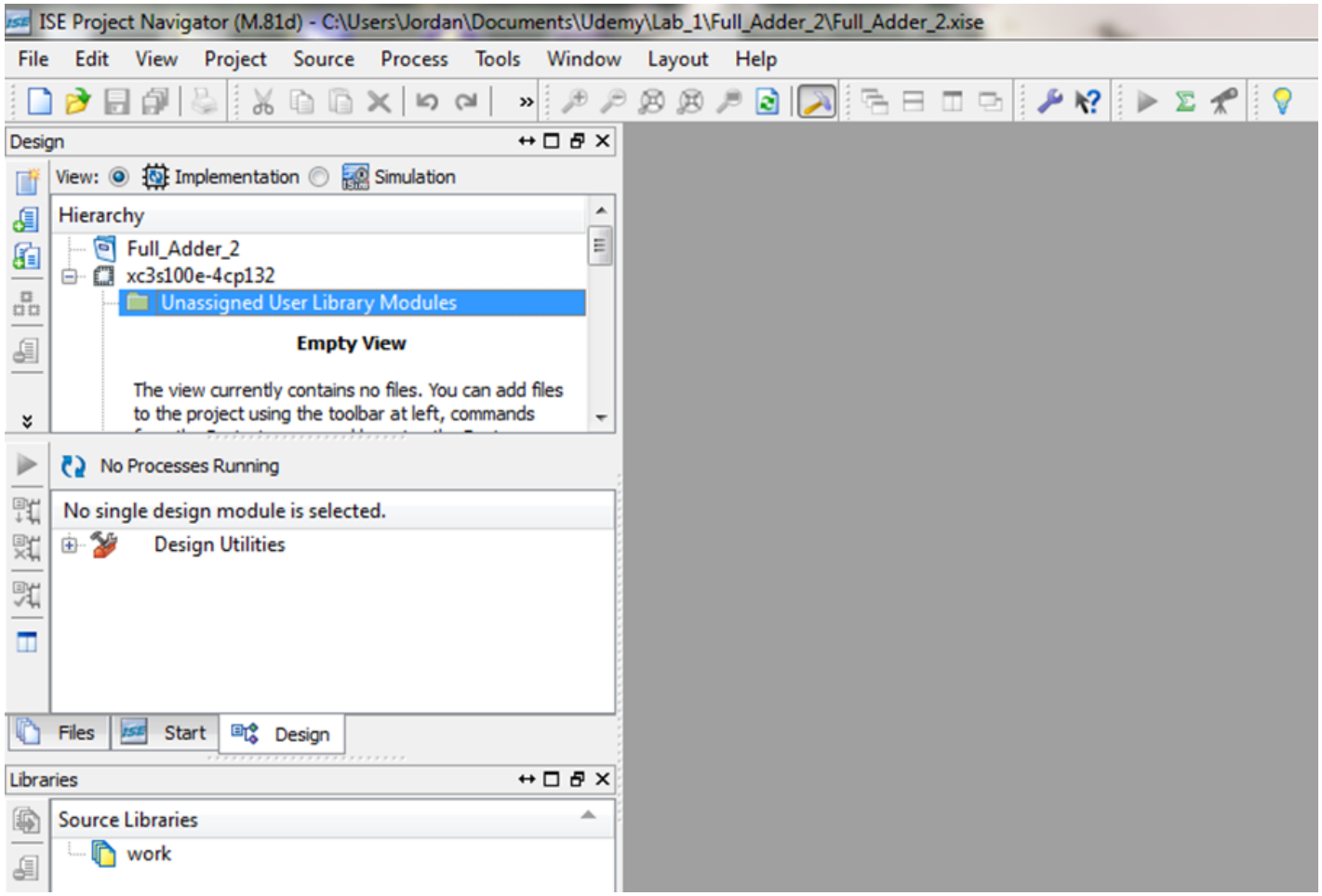


Project Summary

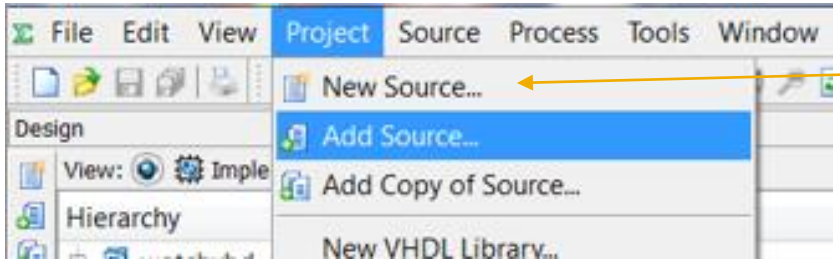


Add Design file

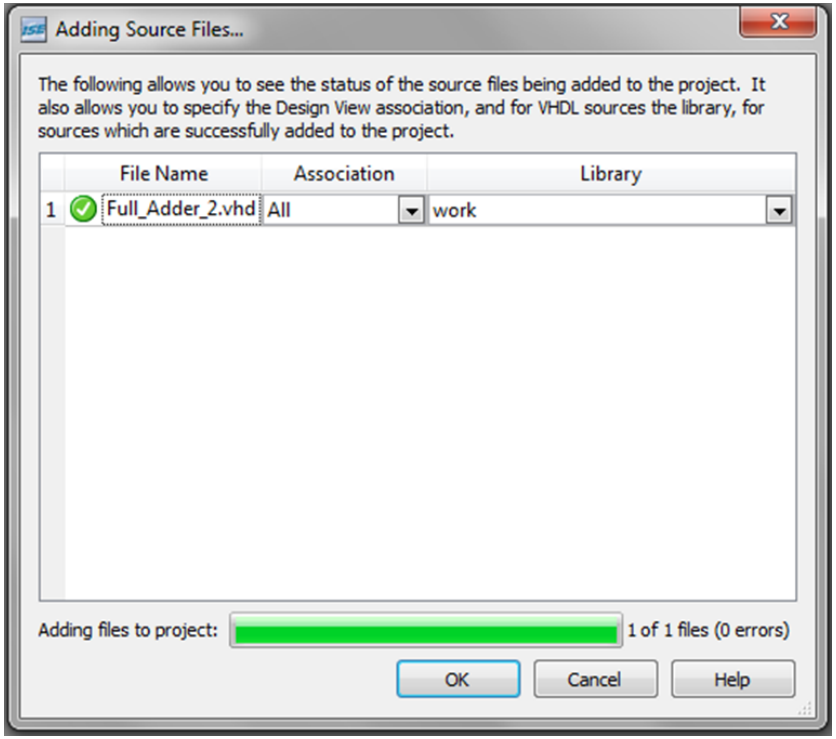
Note: Implementation radio button is selected



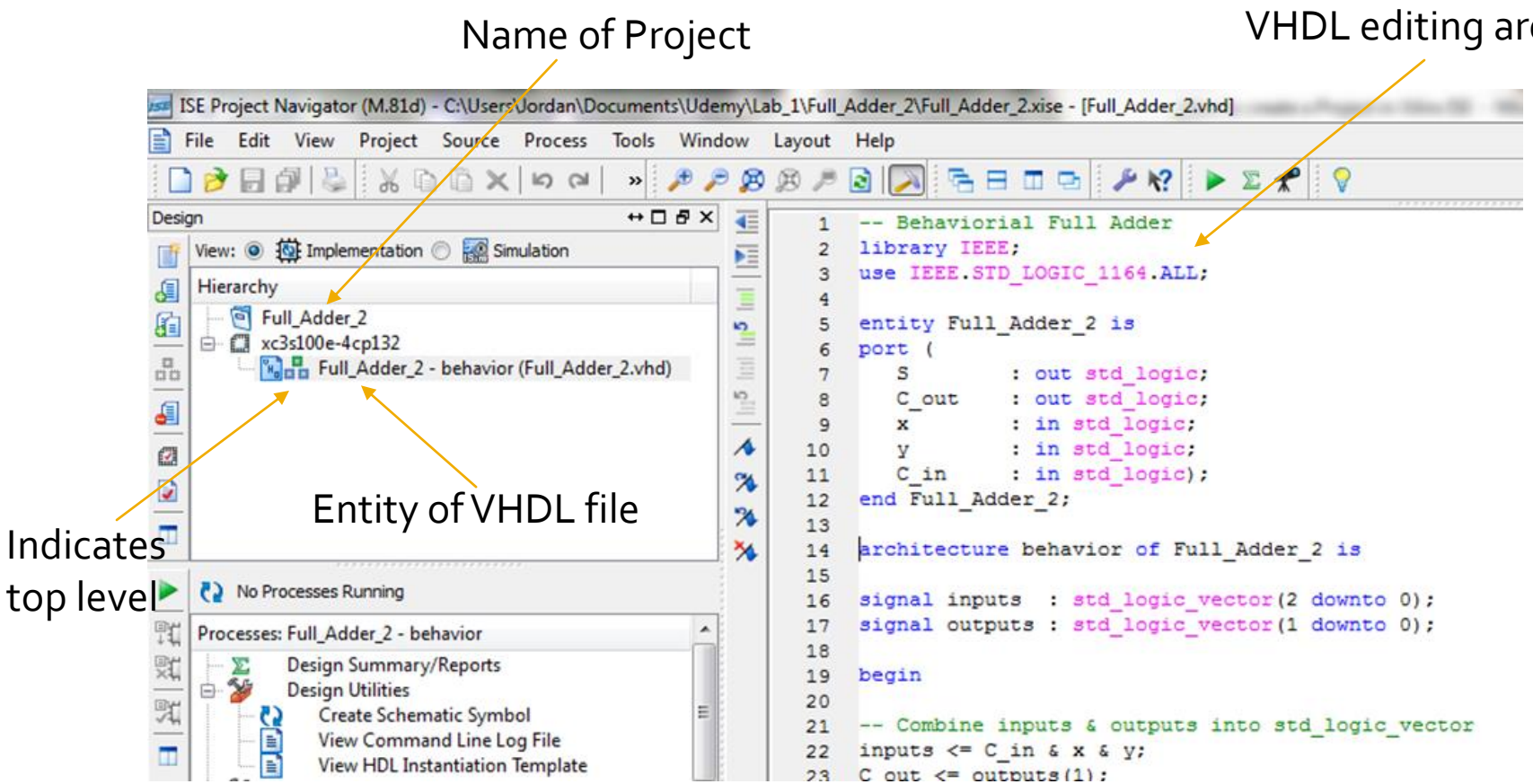
Add Design file



Select "New Source" if you Want to code your VHDL file Inside of Xilinx ISE

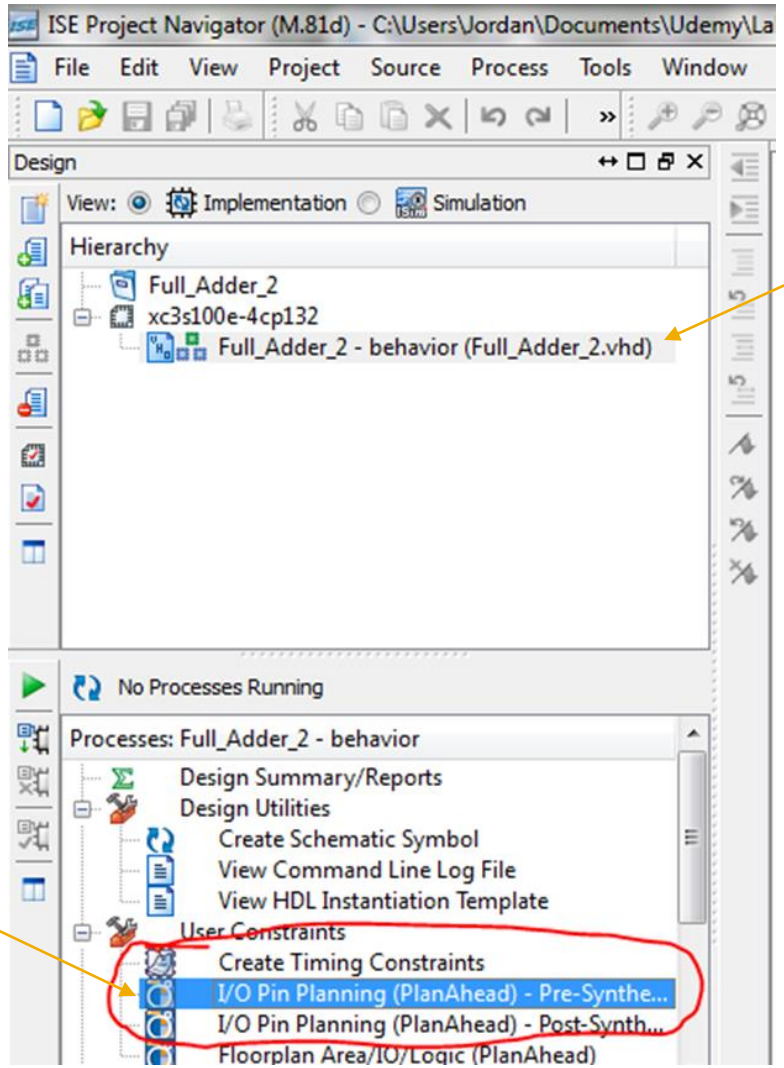


Full_Adder_2 example



Map the I/O

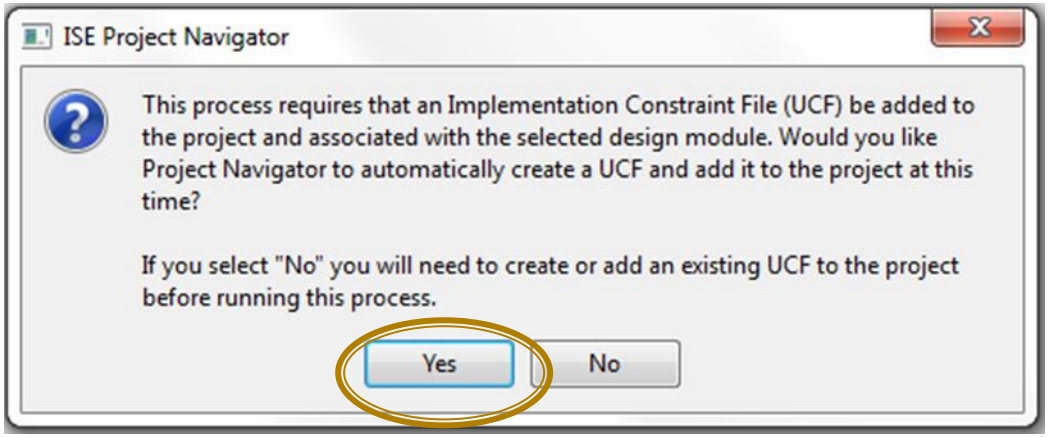
NOTE:
For the labs in this course I will be providing you with the UCF (user constraints file). You will just need to go to Project → Add source and then select the *.ucf file given to you

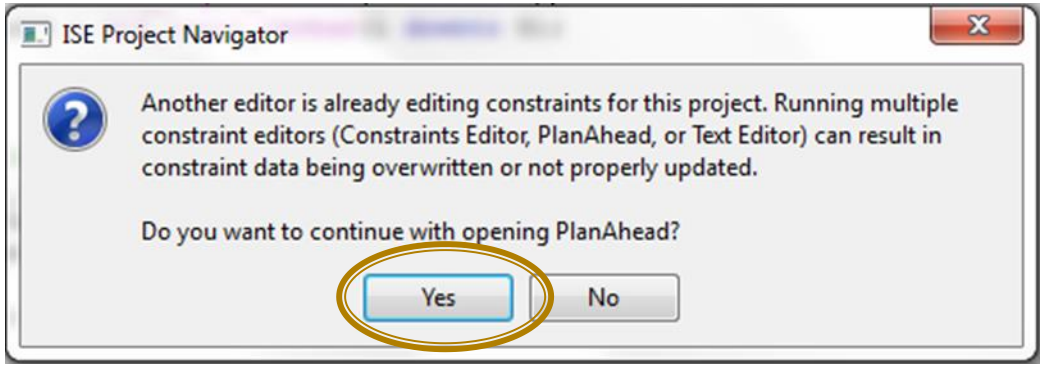


1) Be sure to click on the top level VHDL file to activate it

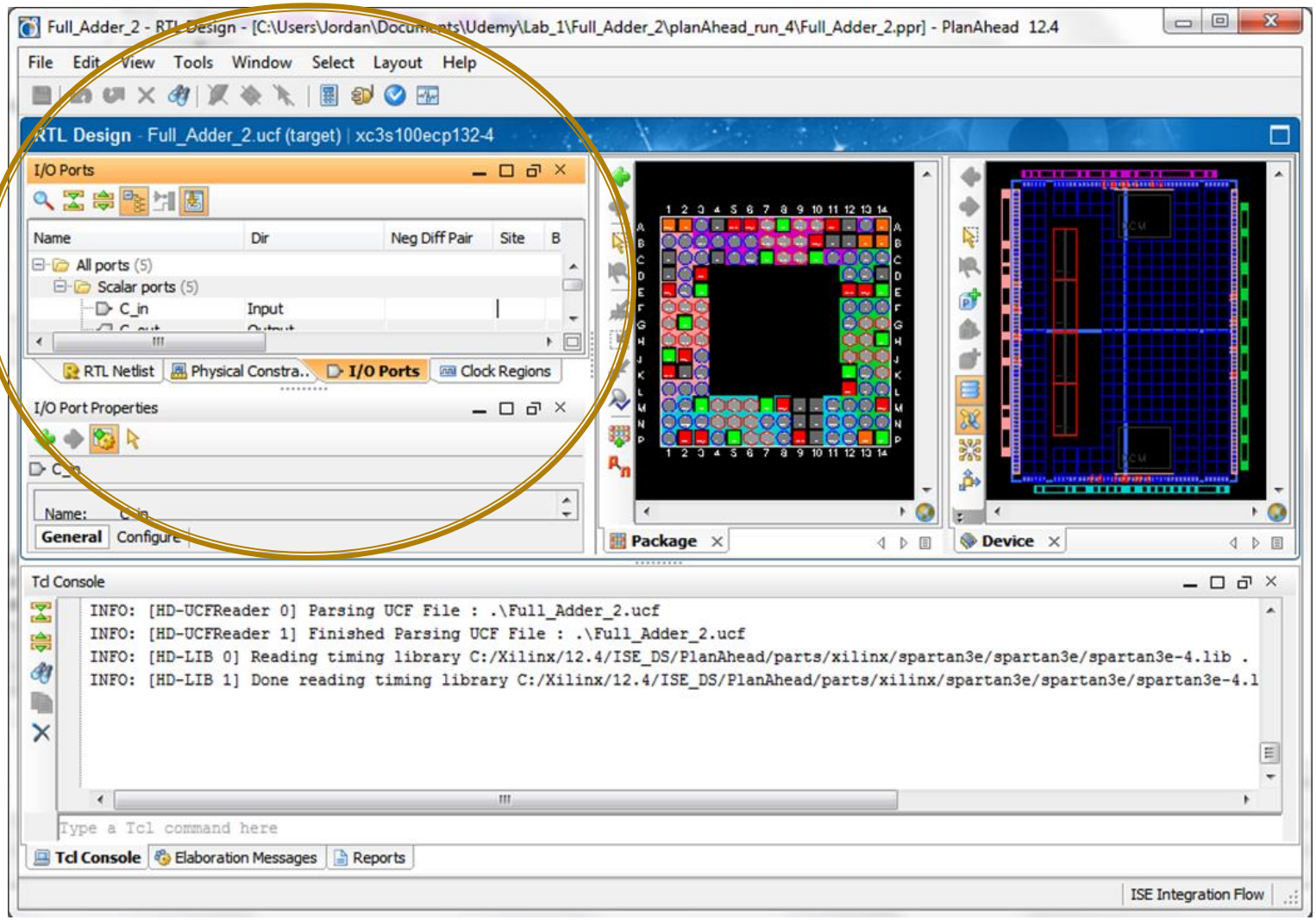
2) Right click. Then select run

Map the I/O

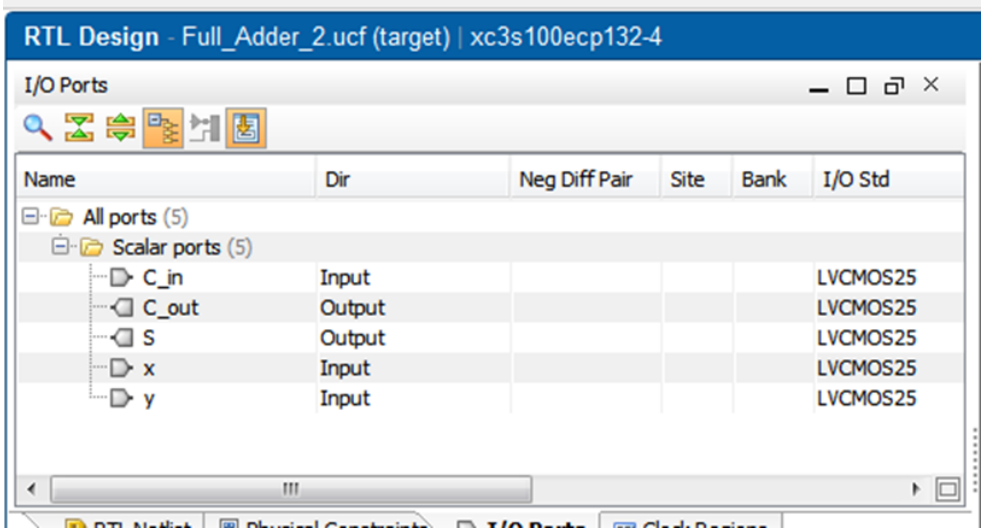

ISE Project Navigator
This process requires that an Implementation Constraint File (UCF) be added to the project and associated with the selected design module. Would you like Project Navigator to automatically create a UCF and add it to the project at this time?
If you select "No" you will need to create or add an existing UCF to the project before running this process.
Yes
No


ISE Project Navigator
Another editor is already editing constraints for this project. Running multiple constraint editors (Constraints Editor, PlanAhead, or Text Editor) can result in constraint data being overwritten or not properly updated.
Do you want to continue with opening PlanAhead?
Yes
No

Plan Ahead


Full_Adder_2 - RTL Design - [C:\Users\Jordan\Documents\Udemy\Lab_1\Full_Adder_2\planAhead_run_4\Full_Adder_2.ppr] - PlanAhead 12.4
File Edit View Tools Window Select Layout Help
RTL Design - Full_Adder_2.ucf (target) | xc3s100ecp132-4
I/O Ports
Name Dir Neg Diff Pair Site B
All ports (5)
Scalar ports (5)
C_in Input
RTL Netlist Physical Constra.. I/O Ports Clock Regions
I/O Port Properties
Name:
General Configure
Package
Device
Tcl Console
INFO: [HD-UCFReader 0] Parsing UCF File : .\Full_Adder_2.ucf
INFO: [HD-UCFReader 1] Finished Parsing UCF File : .\Full_Adder_2.ucf
INFO: [HD-LIB 0] Reading timing library C:/Xilinx/12.4/ISE_DS/PlanAhead/parts/xilinx/spartan3e/spartan3e/spartan3e-4.lib .
INFO: [HD-LIB 1] Done reading timing library C:/Xilinx/12.4/ISE_DS/PlanAhead/parts/xilinx/spartan3e/spartan3e/spartan3e-4.1
Type a Tcl command here
Tcl Console Elaboration Messages Reports
ISE Integration Flow

Plan Ahead



Note:
The port members of the Entity are what show up as inputs and outputs in the Plan ahead tool

```
1  -- Behaviorial Full Adder
2  library IEEE;
3  use IEEE.STD_LOGIC_1164.ALL;
4
5  entity Full_Adder_2 is
6  port (
7     S        : out std_logic;
8     C_out    : out std_logic;
9     x        : in std_logic;
10    y        : in std_logic;
11    C_in     : in std_logic);
12 end Full_Adder_2;
13
14 architecture behavior of Full_Adder_2 is
15
16 signal inputs  : std_logic_vector(2 downto 0);
17 signal outputs : std_logic_vector(1 downto 0);
```

Plan Ahead

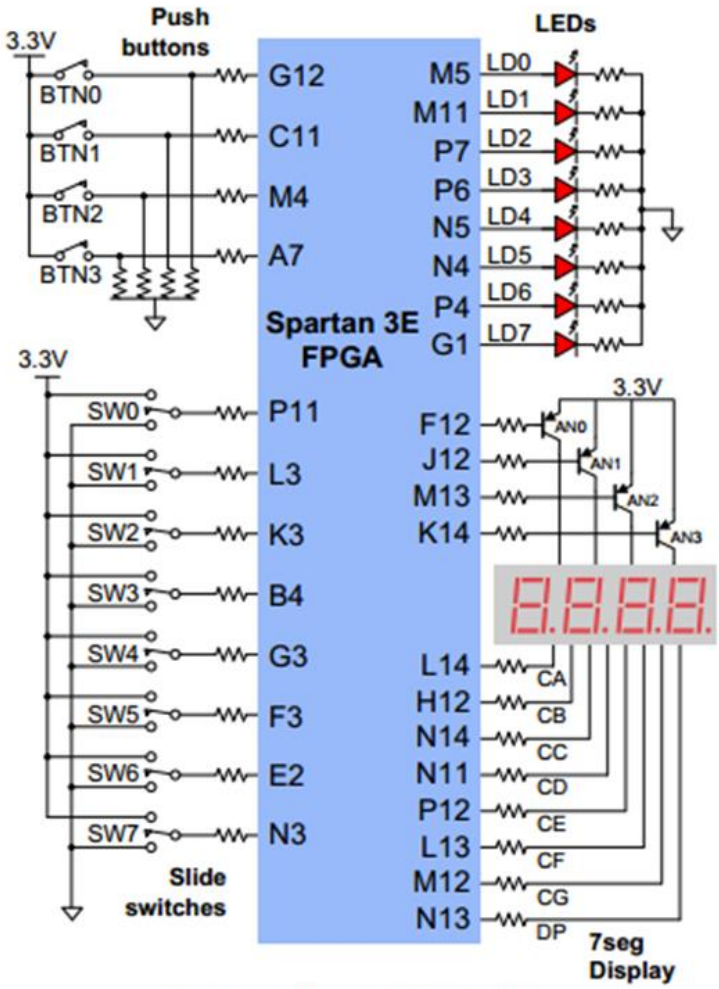
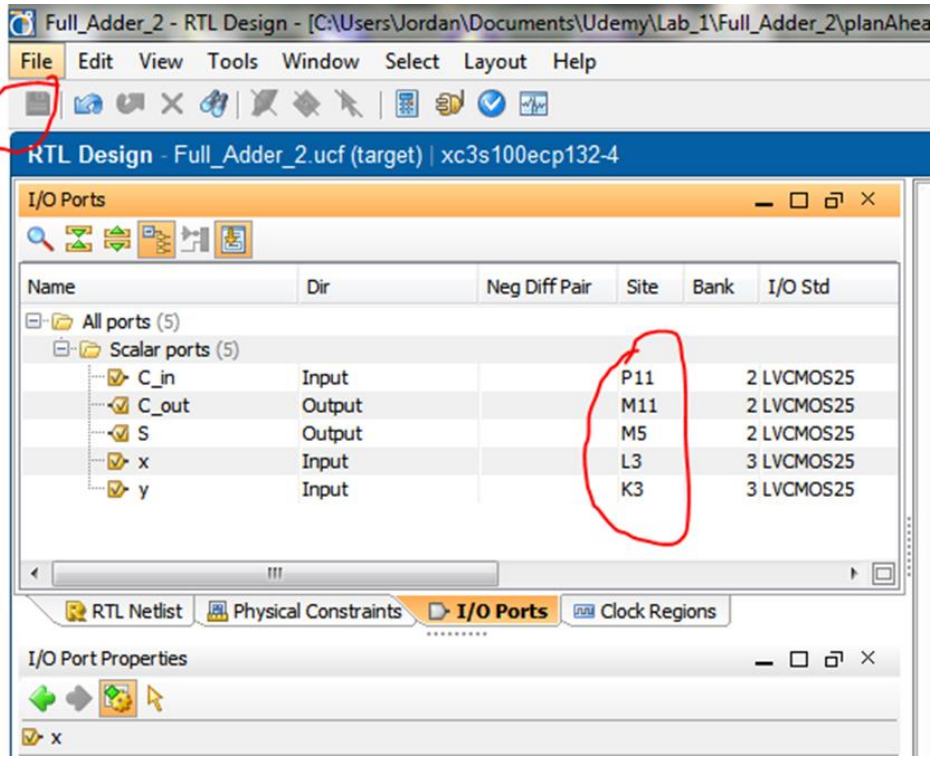
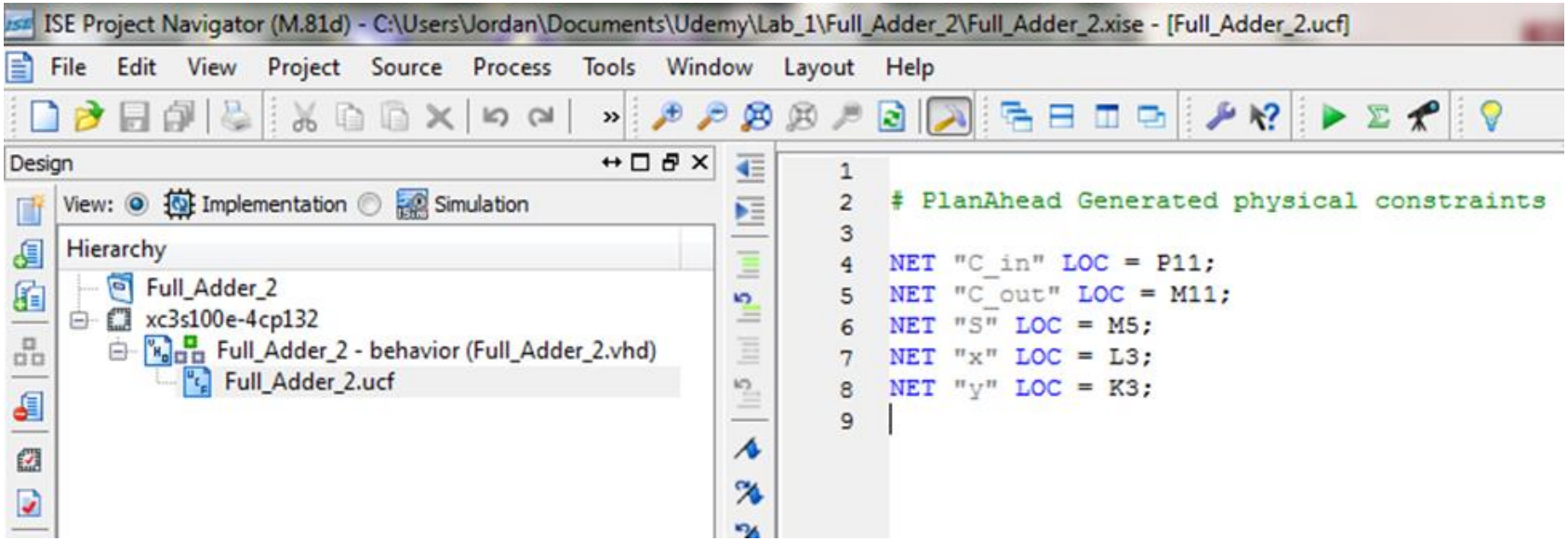


Figure 6. Basys2 I/O circuits

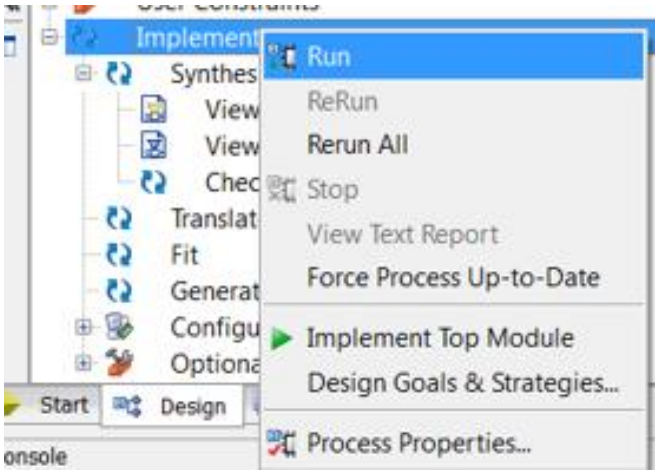


UCF – User Constraints File

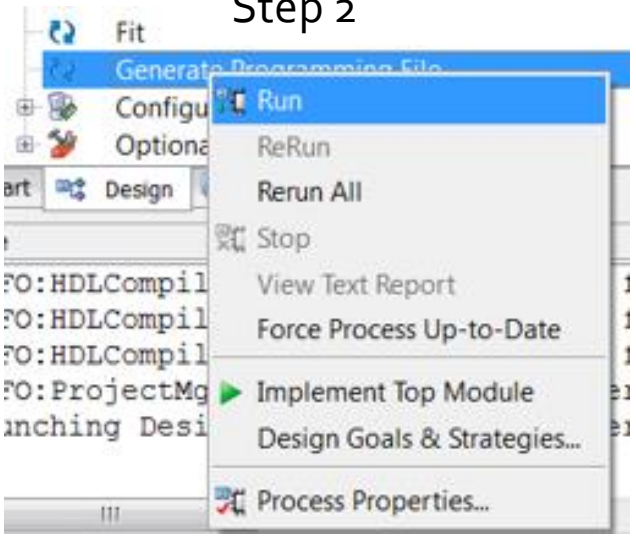


Implement Design & Generate Programming File

Step 1



Step 2



Final file we are wanting

Final Report

Full_Adder_2 Project Status (01/31/2015 - 20:29:14)			
Project File:	Full_Adder_2.xise	**Parser Errors:**	No Errors
Module Name:	Full_Adder_2	**Implementation State:**	Programming File Generated
Target Device:	xc3s100e-4cp132	**• Errors:**	No Errors
Product Version:	ISE 12.4	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	2	1,920	1%	
Number of occupied Slices	1	960	1%	
Number of Slices containing only related logic	1	1	100%	
Number of Slices containing unrelated logic	0	1	0%	
Total Number of 4 input LUTs	2	1,920	1%	
Number of bonded IOBs	5	83	6%	
Average Fanout of Non-Clock Nets	1.60			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:				

Summary

- We can use Plan Ahead inside of Xilinx ISE to create our UCF (User Constraints File)
- You import VHDL files into Xilinx ISE or you can create them using the integrated VHDL editor
- Xilinx ISE is the tool we will be using to generate a programming file to load onto our FPGA (*.bit file)