Module 8.1

Xilinx ISim

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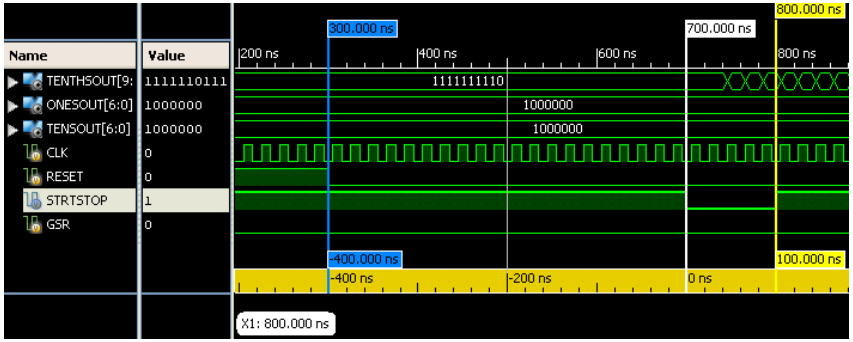
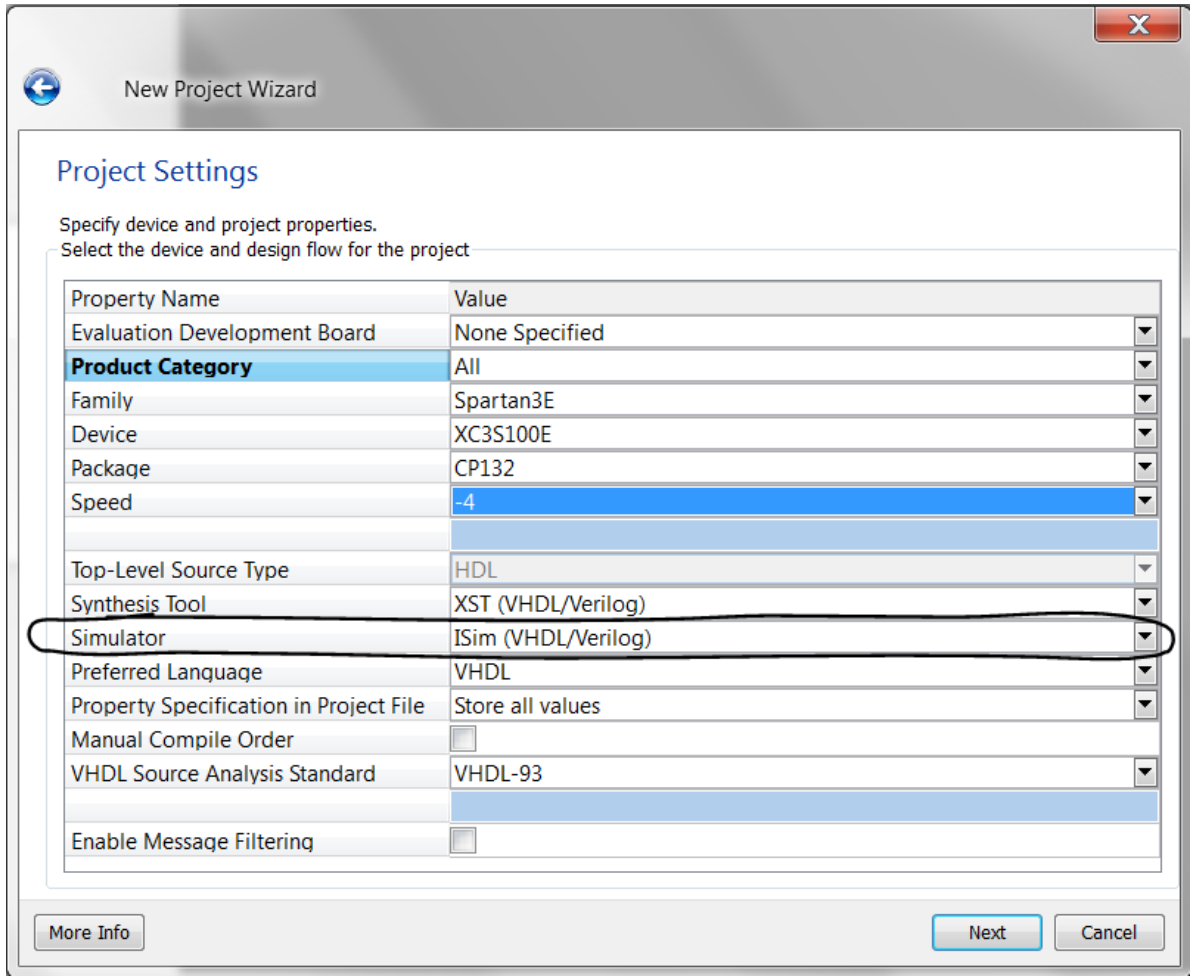
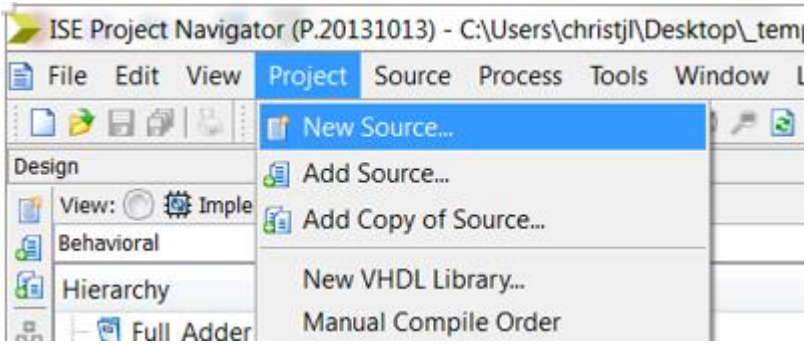
- A simulation tool that is integrated into Xilinx's ISE tool
- Generates waveforms for you to verify the functionality of your VHDL design
- We will be using ModelSim in order to give you exposure to Altera tools



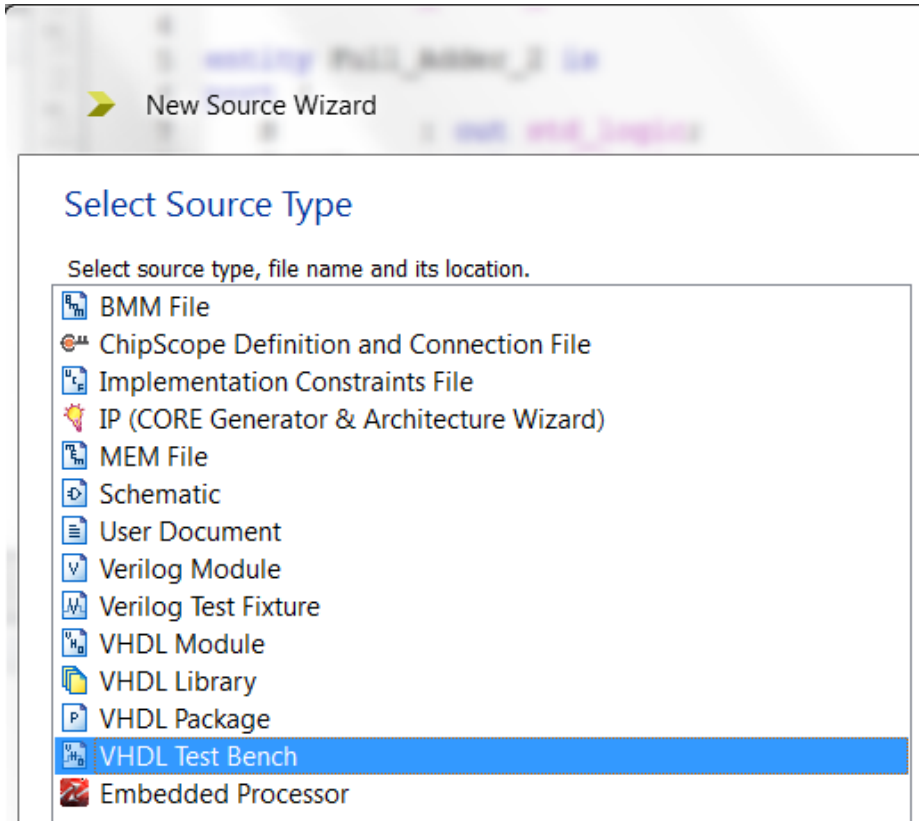
Creating an ISim simulation



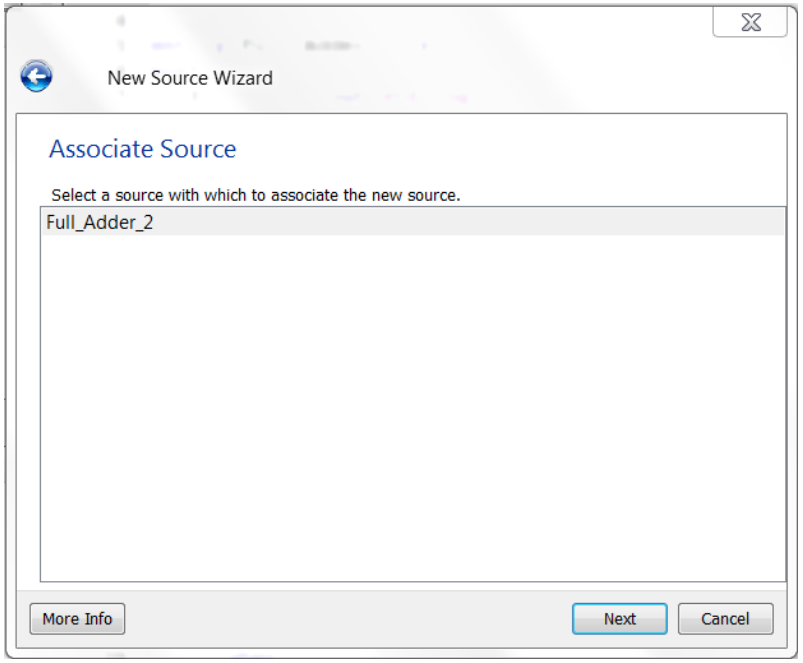
Add Test Bench

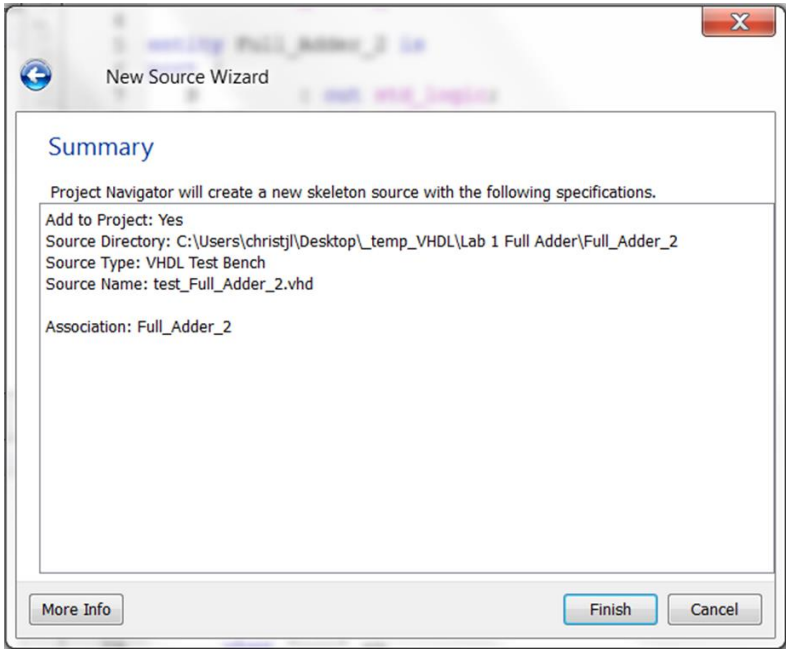


Project → New Source → VHDL Test Bench

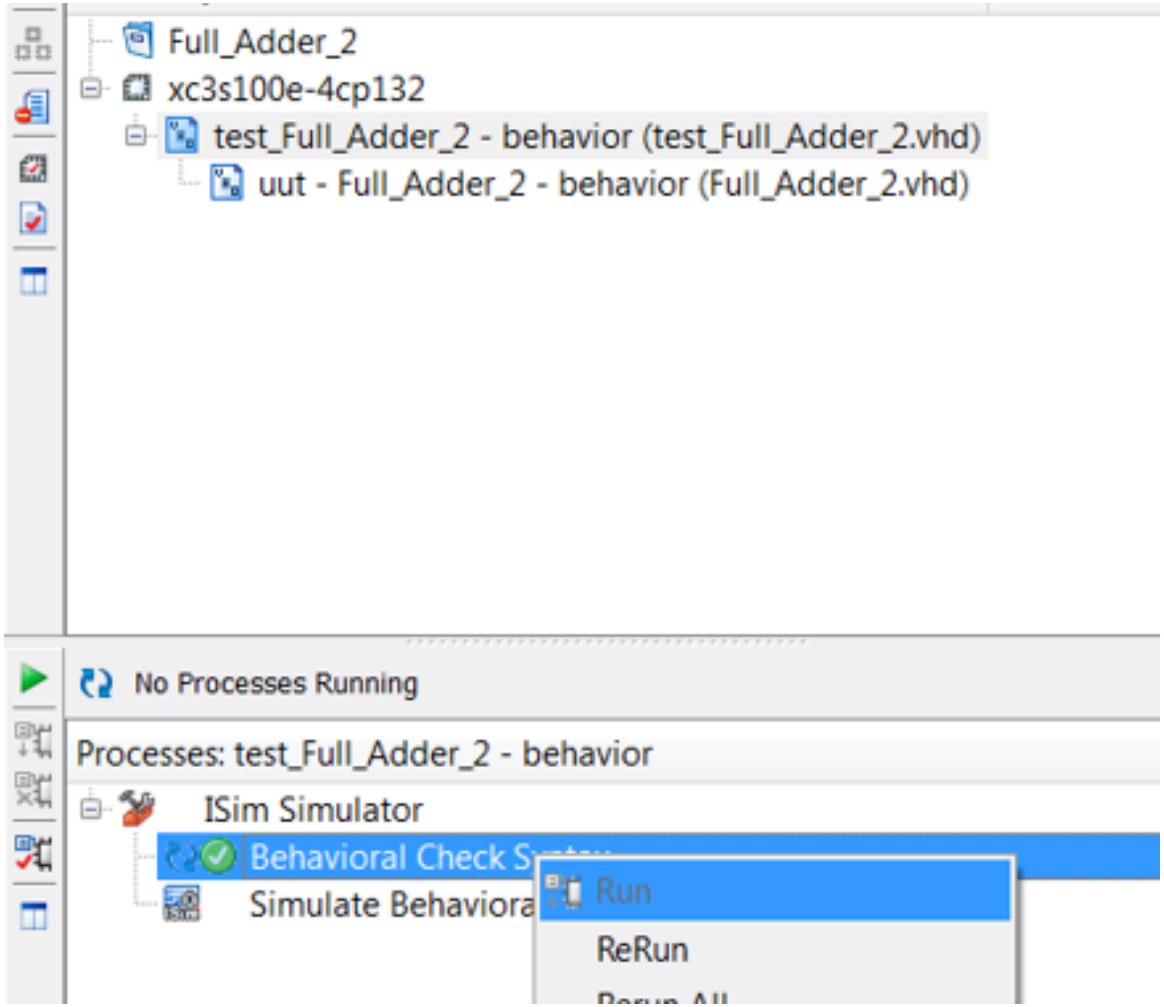


Associate Design File





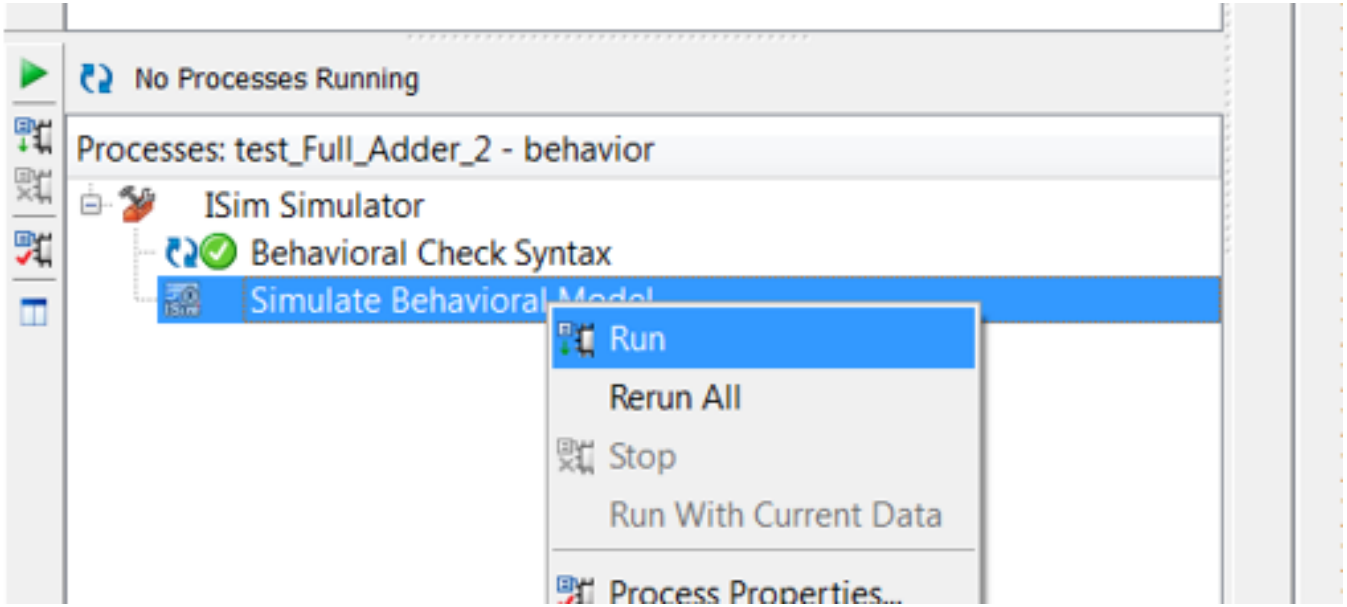
Check Syntax



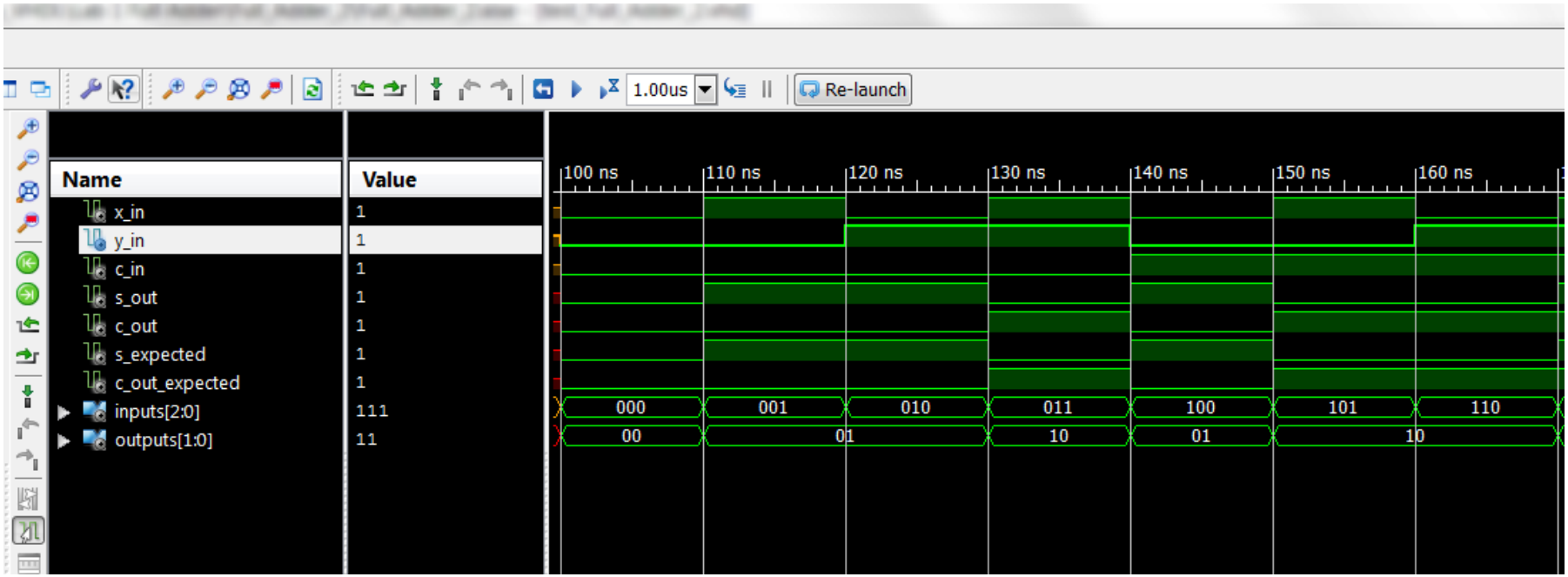
Insert Stimulus

- Insert stimulus that will apply a stimulus to the inputs on your VHDL design
- Check syntax again to be sure your test bench doesn't contain any errors

Run your simulation



Verify Results



Summary

- Isim is a VHDL simulation tool that Xilinx provides
- You can directly integrate your Isim simulation projects with your ISE design