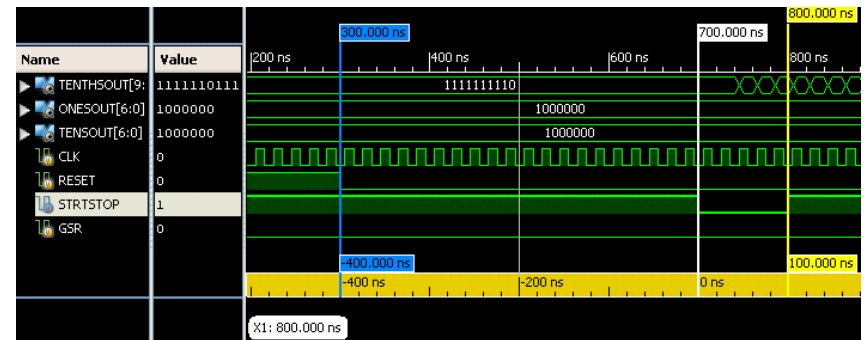


Module 8.1

Xilinx ISim

Xilinx ISim

- A simulation tool that is integrated into Xilinx's ISE tool
- Generates waveforms for you to verify the functionality of your VHDL design
- We will be using ModelSim in order to give you exposure to Altera tools



Creating an ISim simulation

New Project Wizard

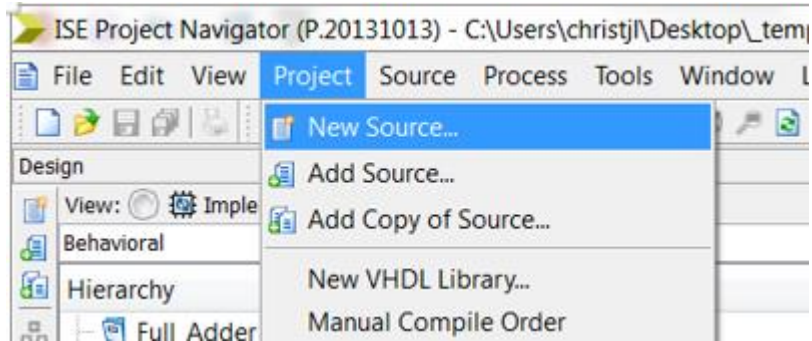
Project Settings

Specify device and project properties.
Select the device and design flow for the project

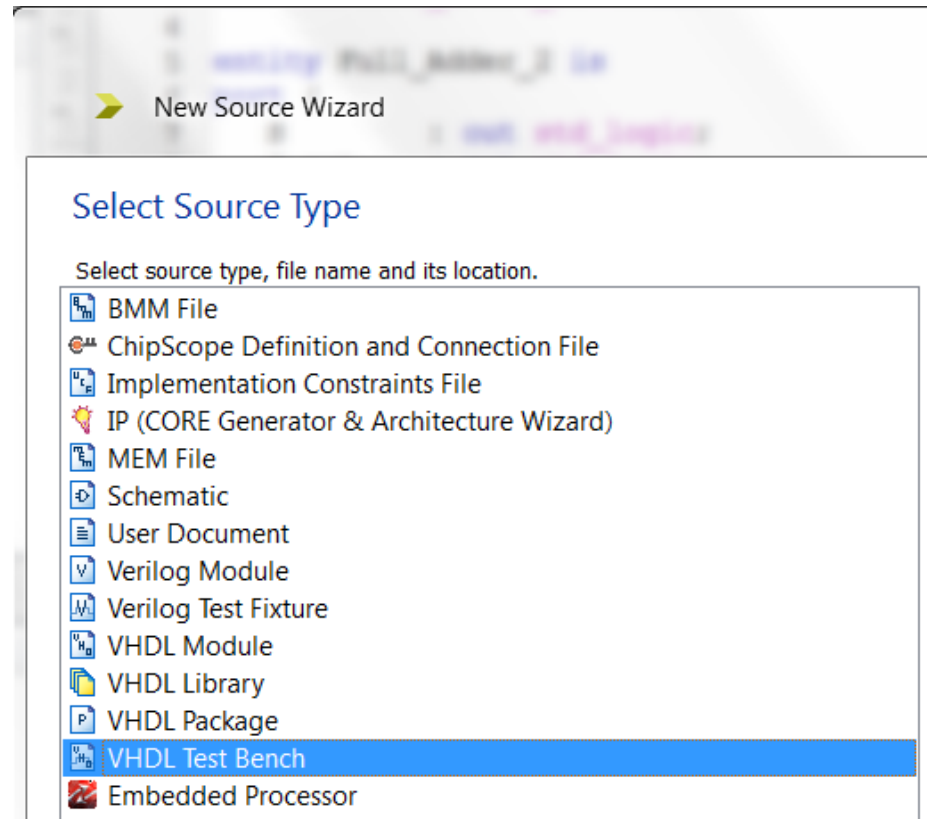
Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3E
Device	XC3S100E
Package	CP132
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

[More Info](#) [Next](#) [Cancel](#)

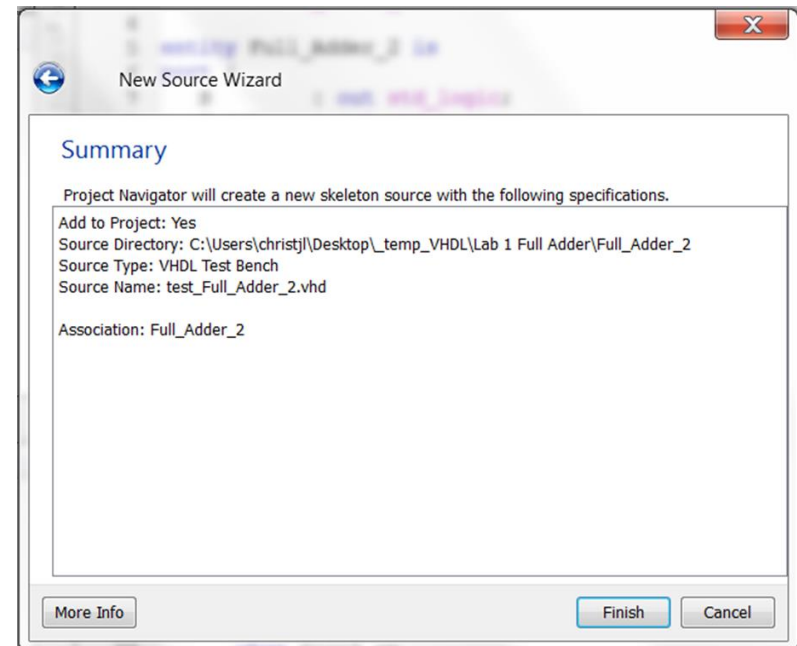
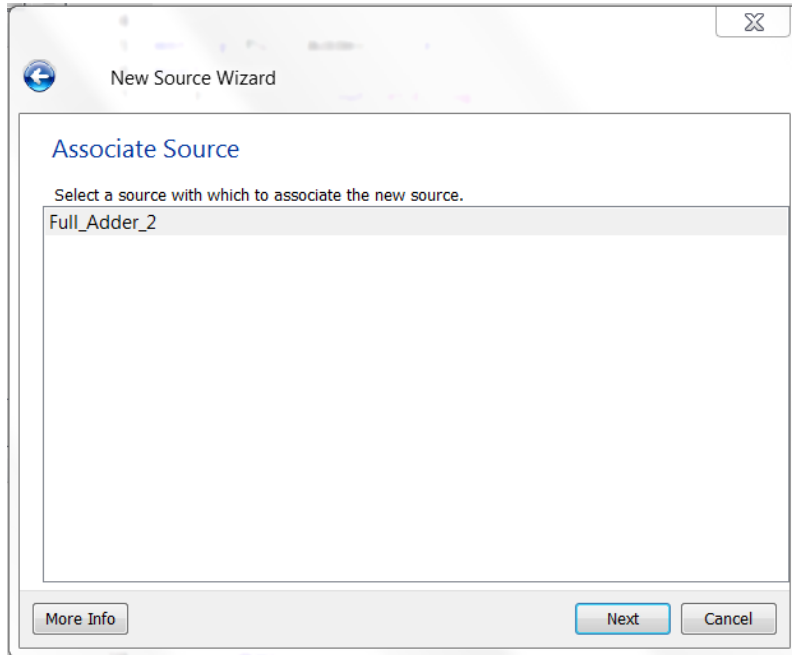
Add Test Bench



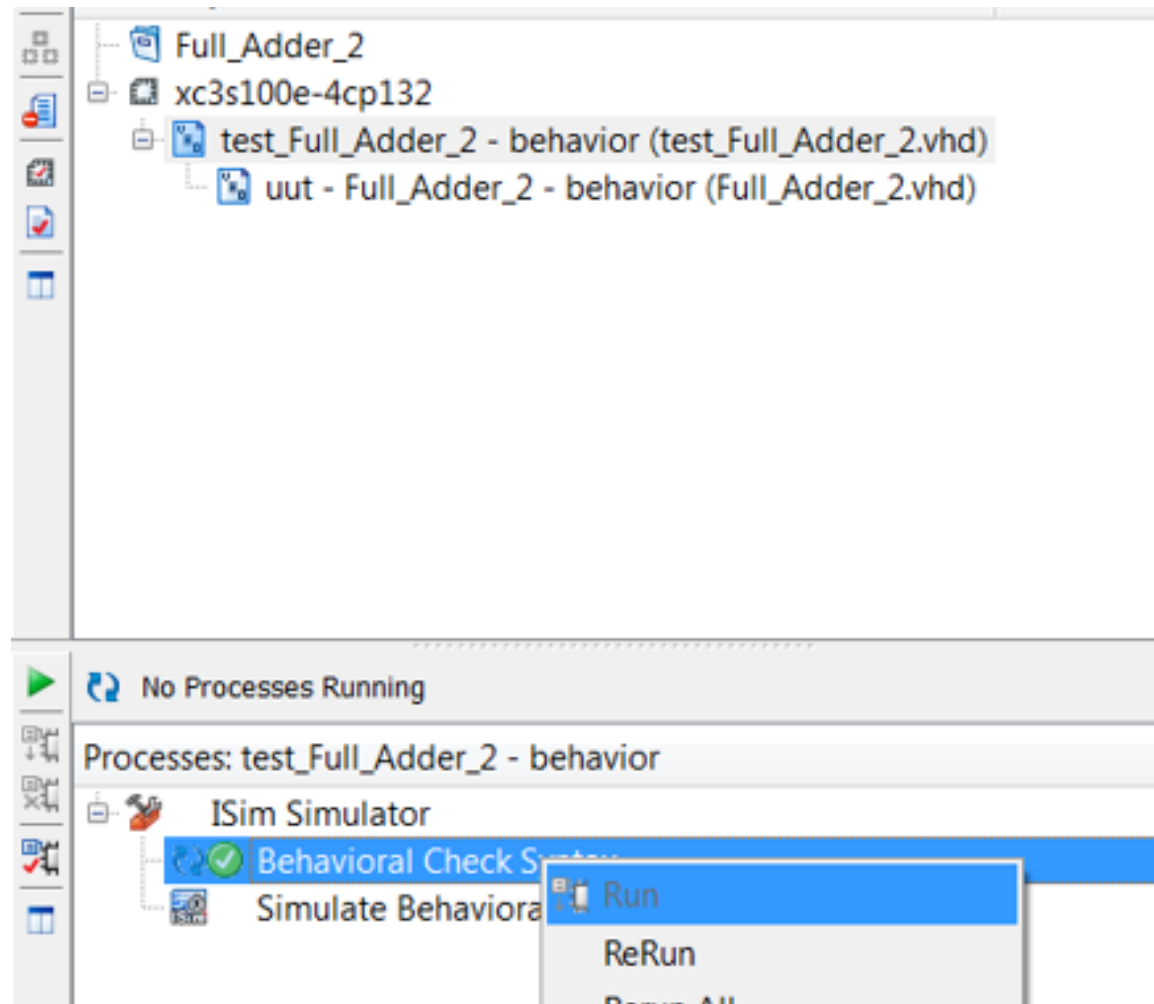
Project → New Source → VHDL Test Bench



Associate Design File



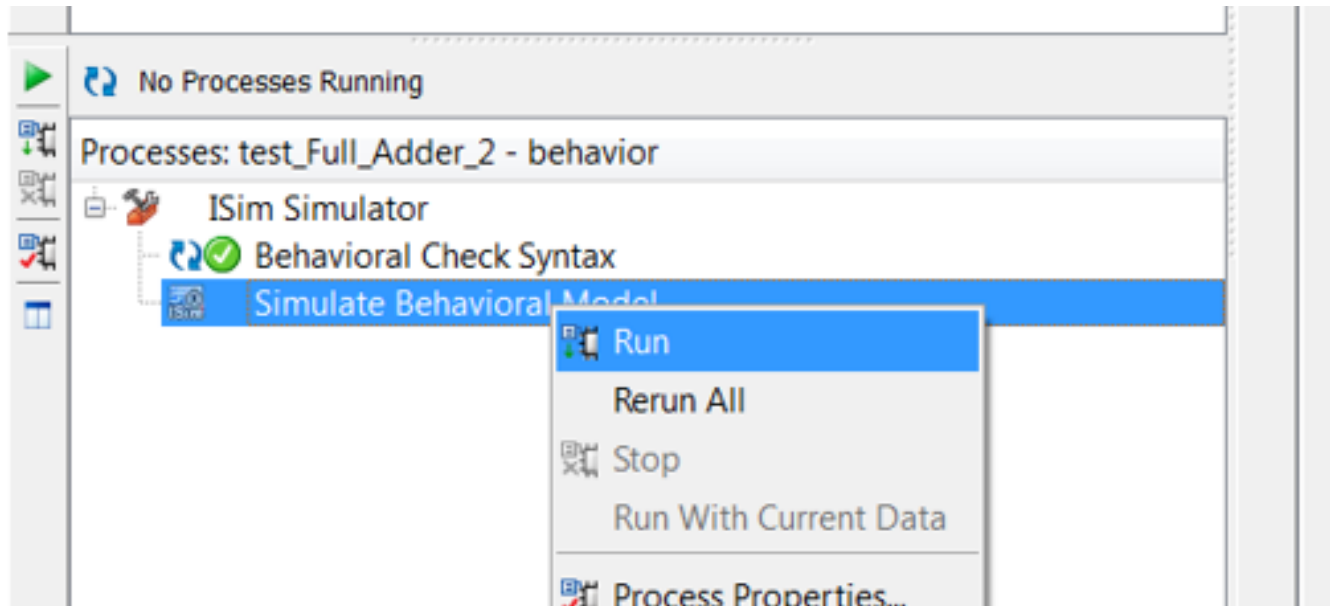
Check Syntax



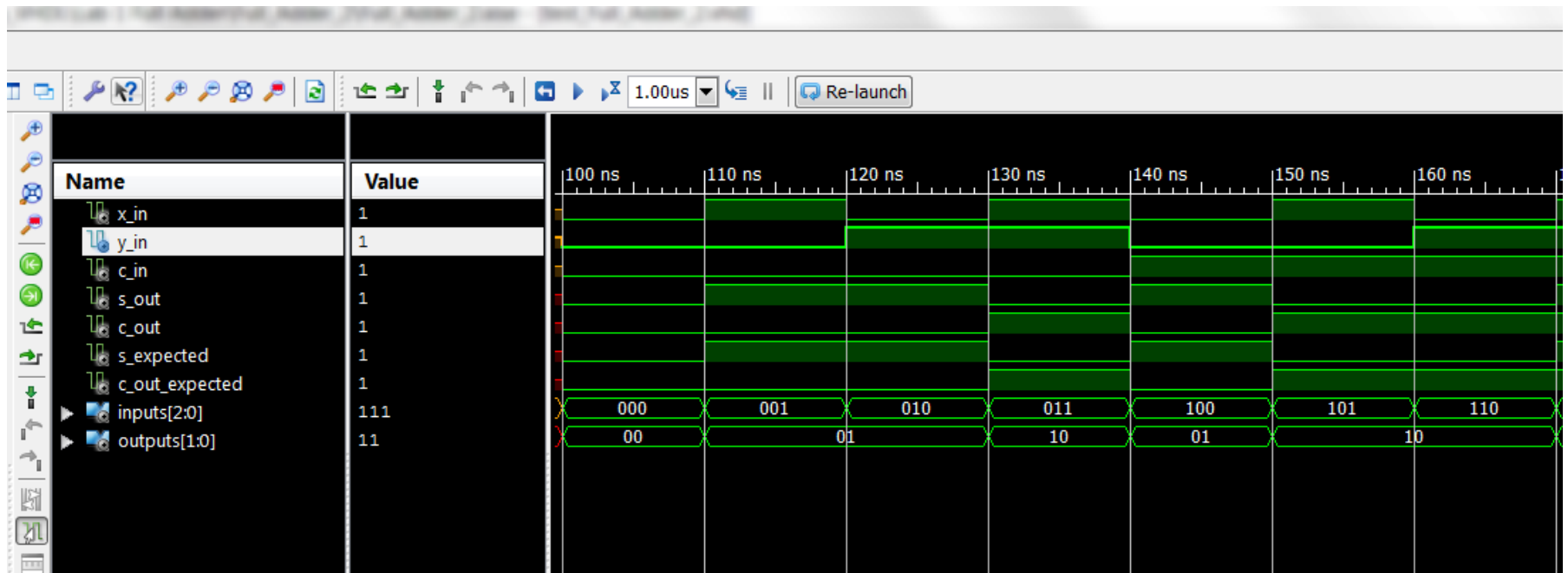
Insert Stimulus

- Insert stimulus that will apply a stimulus to the inputs on your VHDL design
- Check syntax again to be sure your test bench doesn't contain any errors

Run your simulation



Verify Results



Summary

- Isim is a VHDL simulation tool that Xilinx provides
- You can directly integrate your Isim simulation projects with your ISE design