Lab 6

Multiplier

Multiplication in FPGAs

- Not all FPGA's contain dedicated multiplication elements
- Typically your multiplication elements are used to speed up DSP functionality
  - DSP (Digital Signal Processor)

- The Spartan 3E FPGA we have on the BASYS 2 board contains 4 18 bit dedicated multipliers
- We can create our own multiplier through the use of shifting and adding

Binary Multiplication

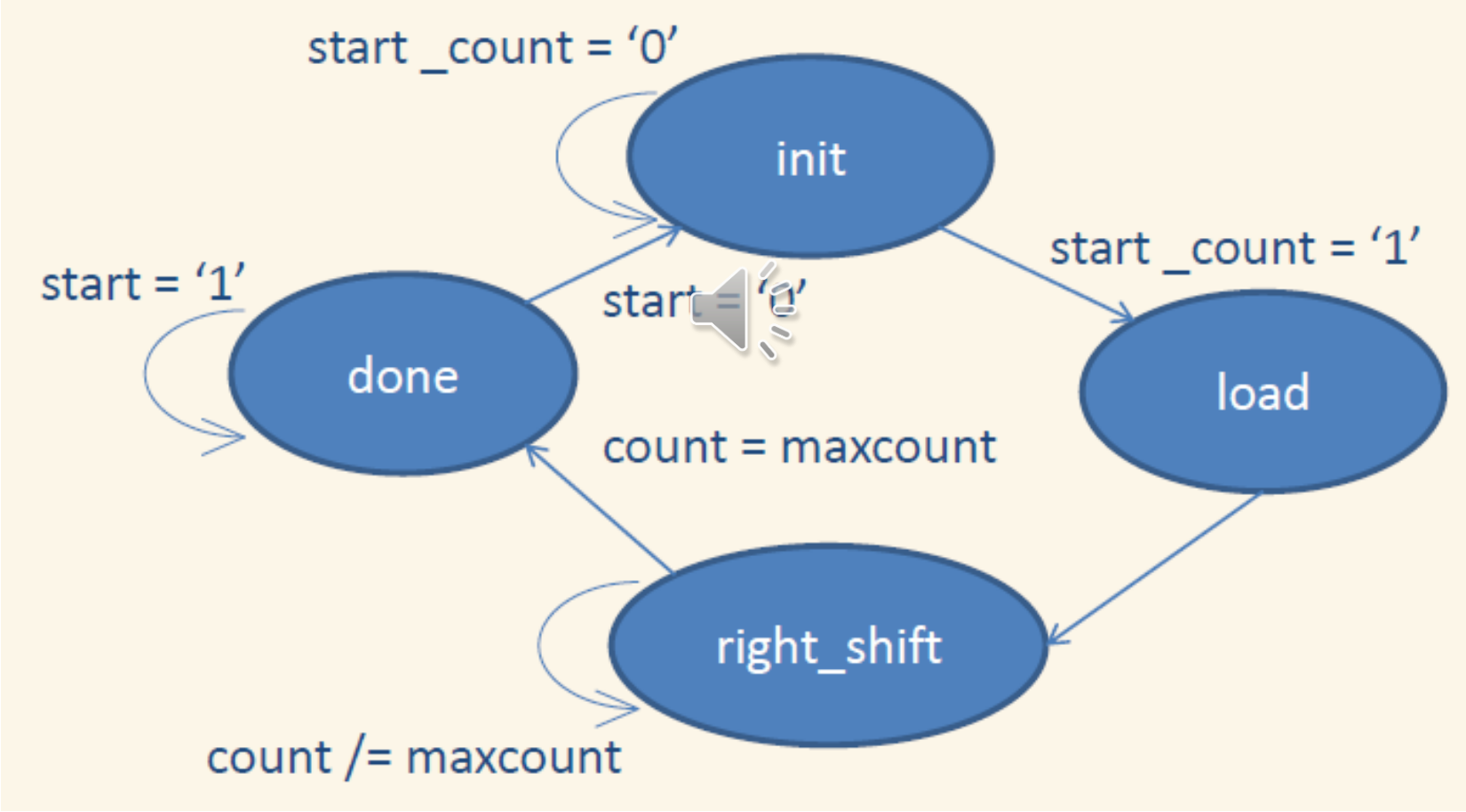
DECIMAL EXAMPLE

```
  12
 x13
  36
+12
 156
```

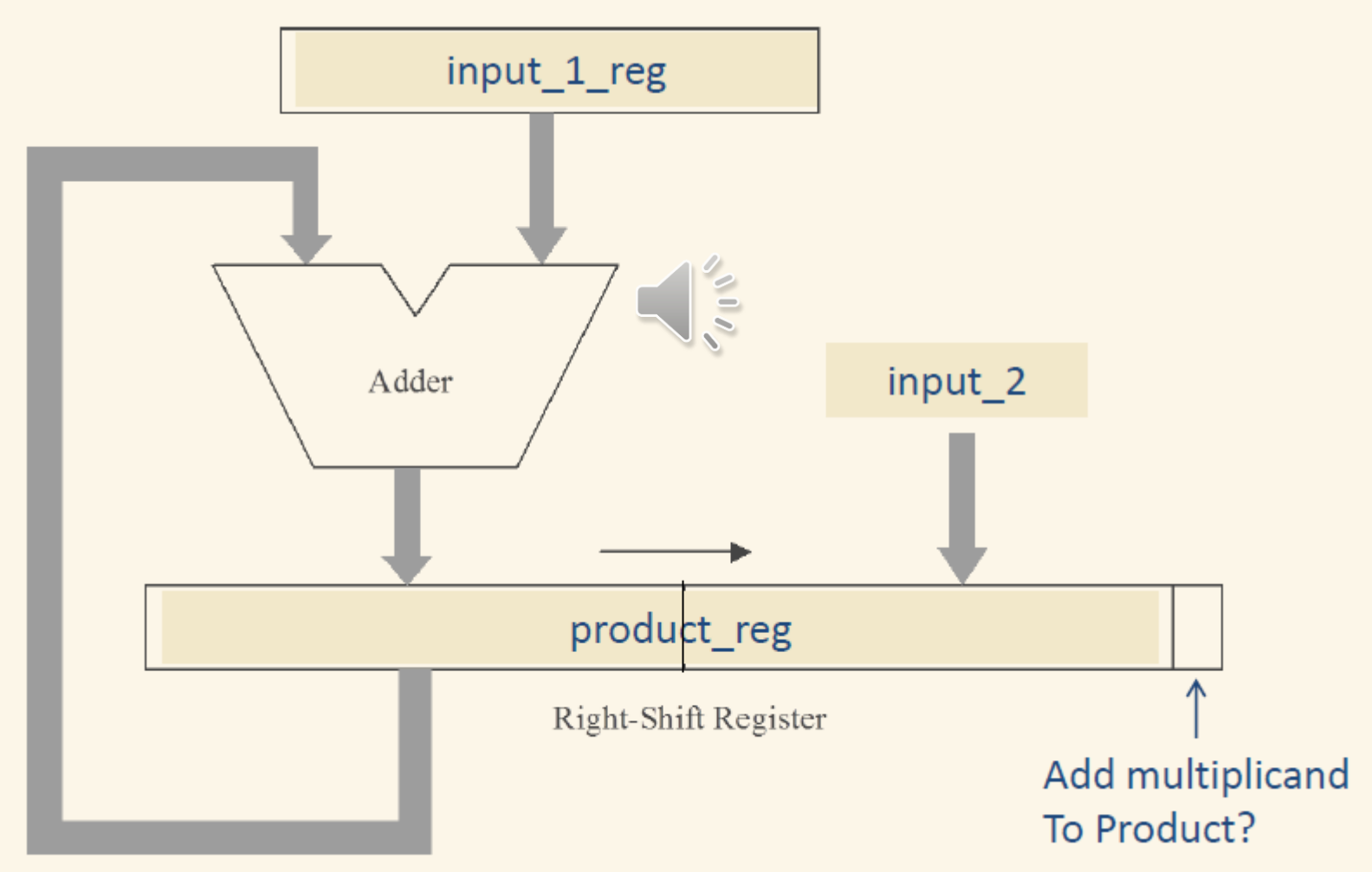
BINARY EXAMPLE

```
     01100
    x01101
     01100
    00000
   01100
  01100
+ 00000
  010011100
```

Multiplier State Machine



Multiplier State Diagram



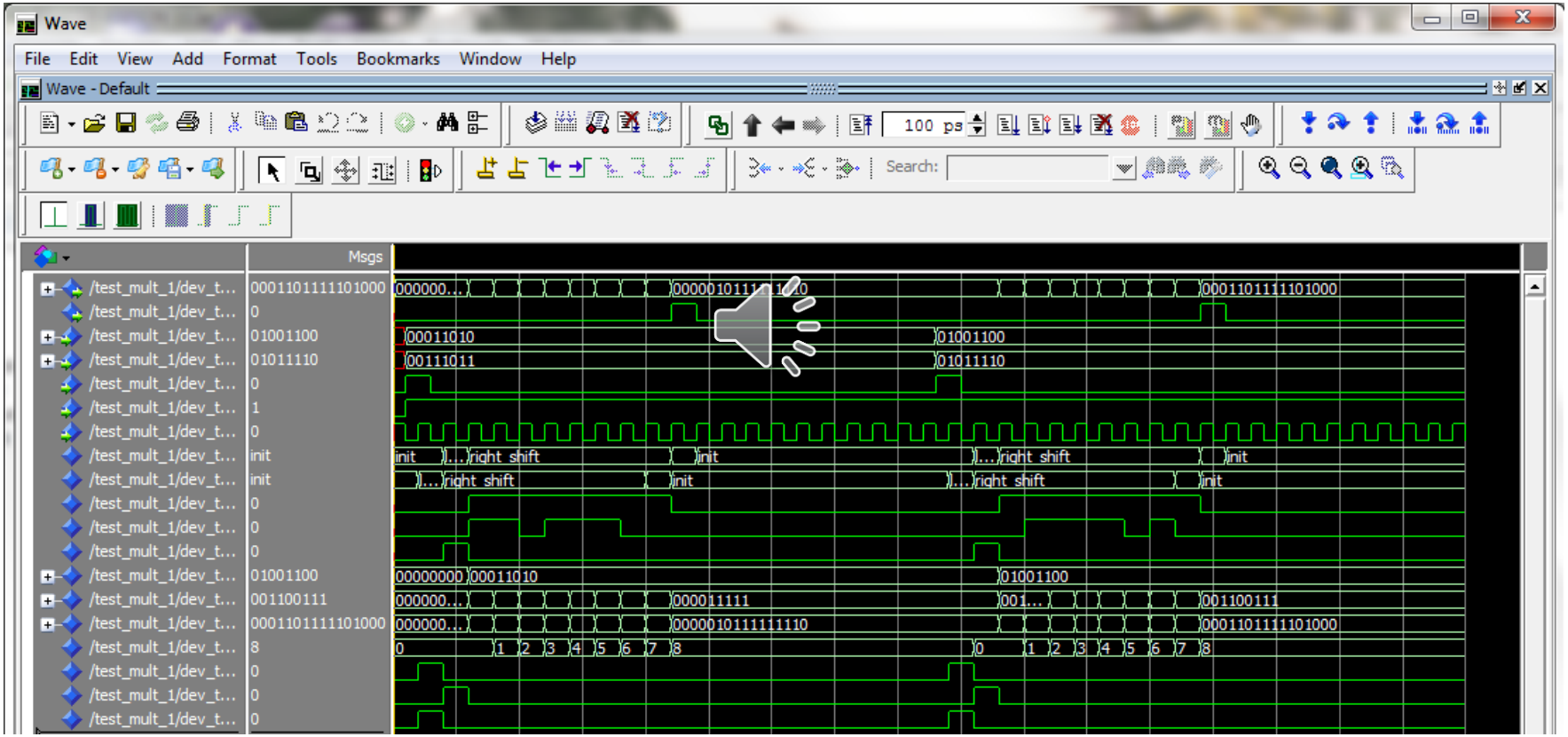
Multiplier Operation

5 Bit Multiplier Example

Iteration	input_1	product_reg	Description
0	01100	00000 01101	Look at LSB, Add and Shift
1	01100	00110 00110	Look at LSB, Shift
2	01100	00011 00011	Look at LSB, Add and Shift
3	01100	00111 10001	Look at LSB, Add and Shift
4	01100	01001 11000	Look at LSB, Shift
5	01100	00100 11100	Result

- Notice that a 5 bit operation has 5 iterations (0 thru 4) the final iteration is the result
- We are designing a 4 bit multiplier so we'll have 4 iterations (0 thru 3) this is so we can display this on our BASYS 2 board

ModelSim Simulation



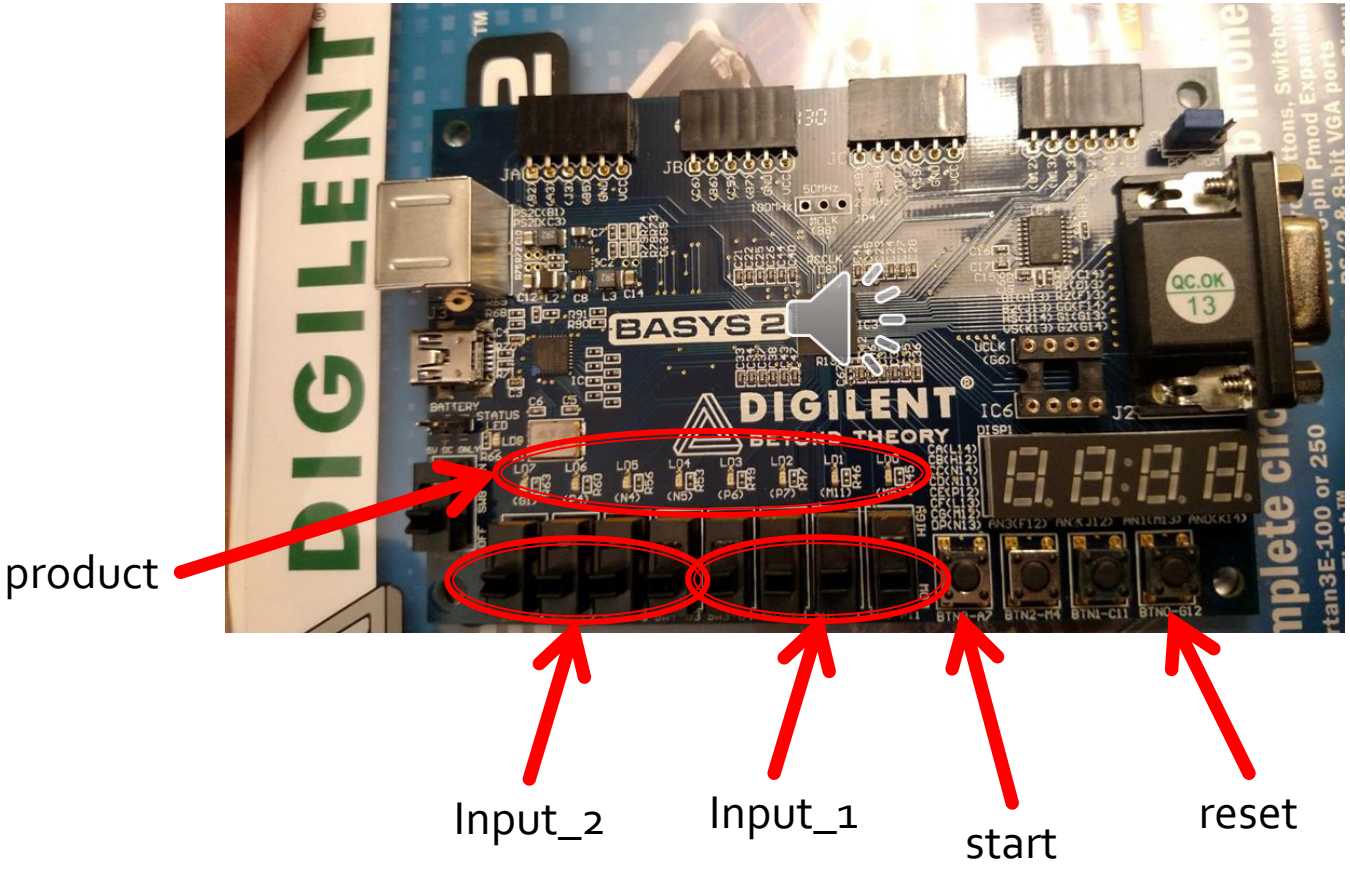
Transcript

```
# Loading work.mult_1(behavior)
# ** Note: SUCCESS!!!  multiplier Test Completed
#    Time: 850 ns  Iteration: 0  Instance: /test_mult_1
```

Tasks

- Complete the Mult_1.vhd design utilizing the state machine
- Simulate your completed design on Modelsim
- Implement your completed design using Xilinx ISE and run it on your BASYS 2 board
  - Note you will have to modify the (*.ucf) file

UCF pin mapping



Outcomes

- Understand how a state machine can be used and implemented
- Become more comfortable with FPGA prototyping
- Understand how to edit a User Constraints File on an FPGA