

1 High-Level Synthesis for FPGA, Part 3: Advanced

Loop-Pipelining (Waveform) Rewinding Pipelined Loops: Quiz
Solution

www.highlevel-synthesis.com

```
#define N 4  
  
void waveform_generator(volatile bool *x) {  
  
    const bool a[N] = {0, 1, 1, 0}; 0110  
  
    for (int i = 0; i <N; i++) {  
#pragma HLS PIPELINE rewind  
        *(x+i) = a[i];  
    }  
}
```