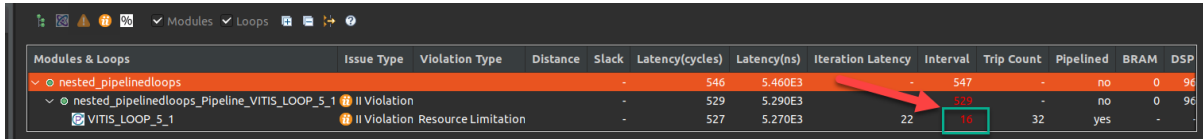


1 High-Level Synthesis for FPGA, Part 3: Advanced

As the pipeline pragma is applied to the outer *for*-loop then, the inner loop will be unrolled automatically.

After synthesis, we will have the following report. In which the initiation interval of the outer loop is 16.



Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP
nested_pipelinedloops					546	5.460E3	-	547	-	no	0	96
nested_pipelinedloops_Pipeline_VITIS_LOOP_5_1	II Violation				529	5.290E3		529		no	0	96
VITIS_LOOP_5_1	II Violation	Resource Limitation			527	5.270E3	22	16	32	yes	-	-