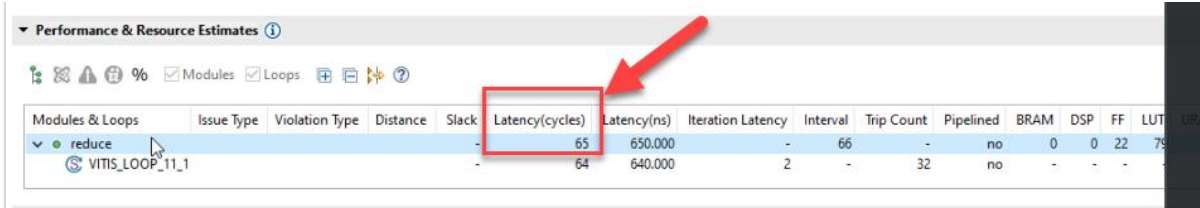


# 1 High-Level Synthesis for FPGA, Part 3: Advanced

Considering the synthesis report, the function latency is 65 and the loop latency is 64.



The screenshot shows a table titled "Performance & Resource Estimates" with the following columns: Modules & Loops, Issue Type, Violation Type, Distance, Slack, Latency(cycles), Latency(ns), Iteration Latency, Interval, Trip Count, Pipelined, BRAM, DSP, FF, and LUT. The table contains two rows: "reduce" and "VITIS\_LOOP\_11\_1". The "Latency(cycles)" column for "reduce" is 65, and for "VITIS\_LOOP\_11\_1" it is 64. A red box highlights the "65" value, and a red arrow points to it from the right.

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT
reduce	-	-	-	-	65	650.000	-	66	-	no	0	0	22	79
VITIS_LOOP_11_1	-	-	-	-	64	640.000	2	-	32	no	-	-	-	-