

# 1 High-Level Synthesis for FPGA, Part 3: Advanced

As can be seen in the following figure.

Write loop latency is  $T1 = 8197 - 8193 = 4 \text{ cycles}$

Write function latency is  $T2 = 8198 - 8193 = 5 \text{ cycles}$

Read loop latency is  $T1 = 8206 - 8198 = 8 \text{ cycles}$

Read function latency is  $T2 = 8206 - 8198 = 9 \text{ cycles}$

These numbers match the result of the Vitis-HLS synthesis reports.

