

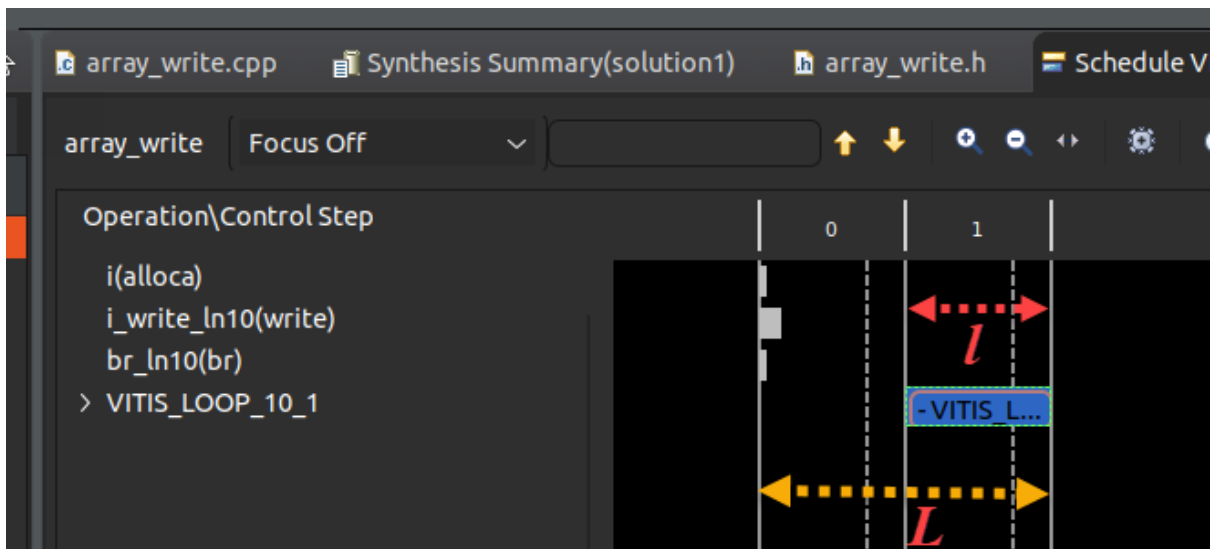
# 1 High-Level Synthesis for FPGA, Part 3: Advanced

## ❖ array\_write

According to the following scheduling diagram, the loop iteration latency is 1 ( $l = 1$ ). As there are four loop iterations, therefore, the total loop latency would be  $4 * 1 = 4$ .

We should add the first cycle to the loop latency to get the total function latency, that is

$$L = 1 + 4 = 5$$



You can see these latencies in the scheduling report below.

The figure shows a screenshot of the 'Performance & Resource Estimates' window. The table below shows the latency values for the 'array\_write' module and its loop iterations. Yellow arrows point to the 'Latency(cycles)' column for 'array\_write' (5) and 'VITIS LOOP 10 1' (4), and to the 'Iteration Latency' column for 'VITIS LOOP 10 1' (1).

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
array_write	-	-	-	-	5	50,000	-	6	-	no	0	0	5	53	0
VITIS LOOP 10 1	-	-	-	-	4	40,000	1	-	4	no	-	-	-	-	-

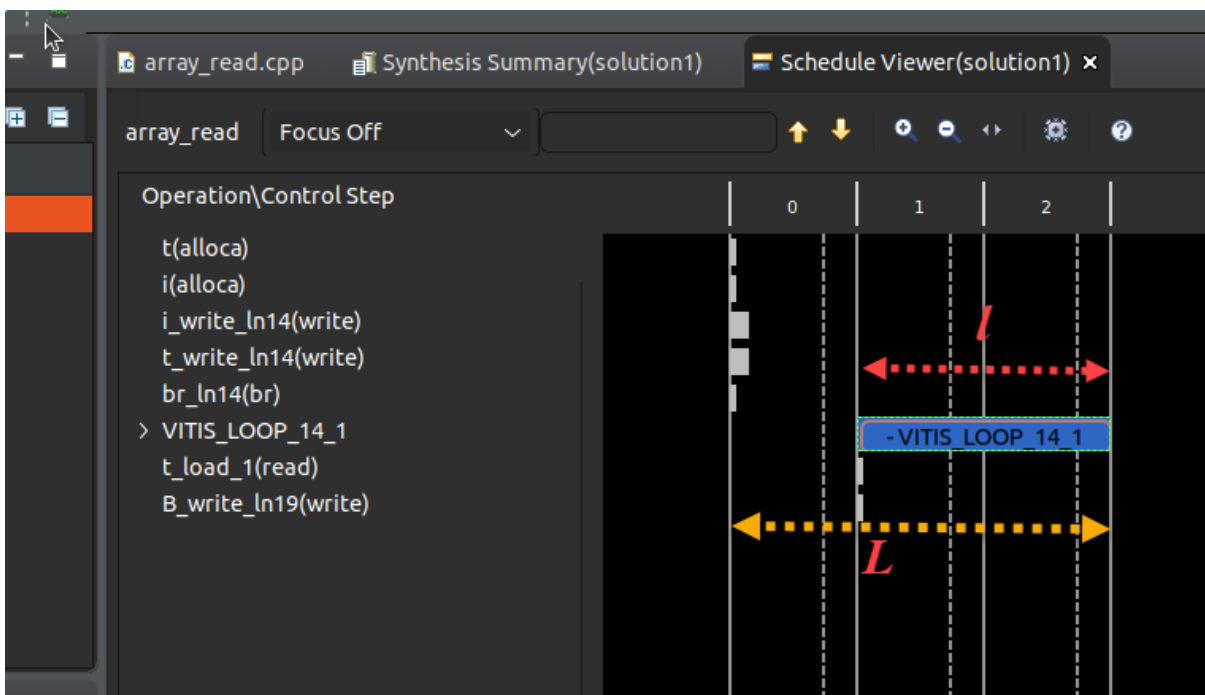
## 2 High-Level Synthesis for FPGA, Part 3: Advanced

### ❖ array\_read

According to the following scheduling diagram, the loop iteration latency is 2 ( $l = 2$ ). As there are four loop iterations, therefore, the total loop latency would be  $4 * 2 = 8$ .

We should add the first sycle to the loop latency to get the total function latency, that is

$$L = 1 + 8 = 9$$



You can see these latencies in the scheduling report below.

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
array_read			-		9	90,000	-	10	-	no	0	0	14	70	0
VITIS LOOP 14 1			-		8	80,000	2	-	4	no	-	-	-	-	-