

1 High-Level Synthesis for FPGA, Part 3: Advanced

If $N = 16$, then the following figures show the synthesis reports. As can be seen, internal arrays are not mapped to BRAM. Instead, shift registers (formed by flip-flops) implement the memories.

Name	BRAM	URAM	Pragma	Variable	Storage	Impl	Latency
vector_addition	-	-					
a_U	-	-		a	ram_1p	auto	1
b_U	-	-		b	ram_1p	auto	1
c_U	-	-		c	ram_1p	auto	1
vector_addition_Pipeline_VITIS_LOOP_7_1	-	-					
vector_addition_Pipeline_VITIS_LOOP_12_2	-	-					
vector_addition_Pipeline_VITIS_LOOP_16_3	-	-					

Utilization Estimates

Summary

Name	BRAM 18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	-	-	-
FIFO	-	-	-	-	-
Instance	-	-	28	211	-
Memory	0	-	96	24	0
Multiplexer	-	-	-	134	-
Register	-	-	9	-	-
Total	0	0	133	369	0
Available	100	90	41600	20800	0
Utilization (%)	0	0	-0	1	0

Detail

Instance

DSP

Memory

Memory	Module	BRAM 18K	FF	LUT	URAM	Words	Bits	Banks	W*Bits*Banks
a_U	a RAM AUTO 1R1W	0	32	8	0	16	32	1	512
b_U	a RAM AUTO 1R1W	0	32	8	0	16	32	1	512
c_U	a RAM AUTO 1R1W	0	32	8	0	16	32	1	512
Total		0	96	24	0	48	96	3	1536

FIFO

Expression

Multiplexer

2 High-Level Synthesis for FPGA, Part 3: Advanced

If $N = 64$, then the following figures show the synthesis reports. As can be seen, internal arrays are mapped to BRAMs.

