

1 High-Level Synthesis for FPGA, Part 3: Advanced

- 1- Note that 19 is a decimal number. The diagram shows the number in hexadecimal. So, 13 is the hexadecimal representation of 19 in decimal.
- 2- As shown in the figure below, the pulse happens at clock 512, and the result appears at clock 769. Therefore, the result is ready after $(769 - 512) * 10ns = 2,570 ns$.

