The valid signal indicates the validity of the data.

The acknowledge signal indicates the consumption of the data.

If the design is ready for input data, but the input valid is Low, the design stalls and waits for the input valid to be asserted to indicate a new input value is present. When the input valid is asserted High, an output acknowledge is asserted High to indicate the data was read.

When an output port is written to, its associated output valid signal is simultaneously asserted to indicate valid data is present on the port.

If the associated input acknowledge is Low, the design stalls and waits for the input acknowledge to be asserted. When the input acknowledge is asserted, indicating the data has been read, the output valid is deasserted on the next clock edge.

Ref. “Vitis High-Level Synthesis User Guide” **UG1399**