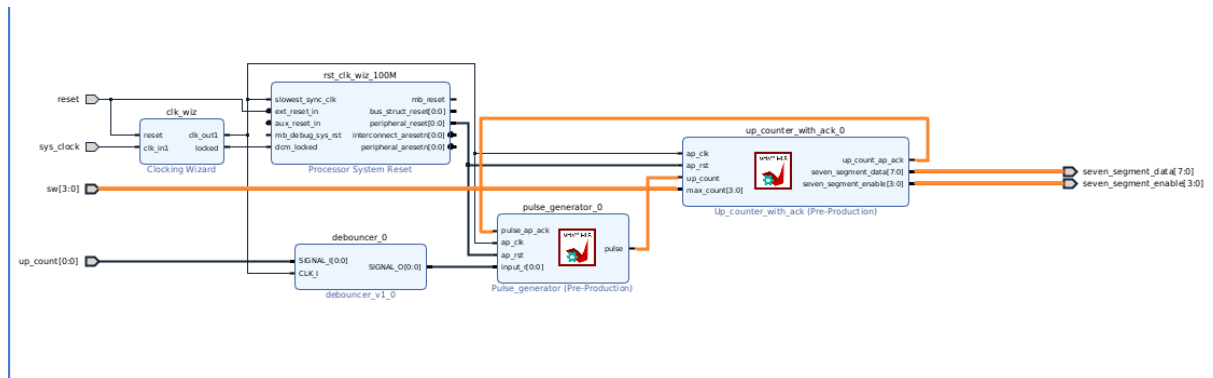
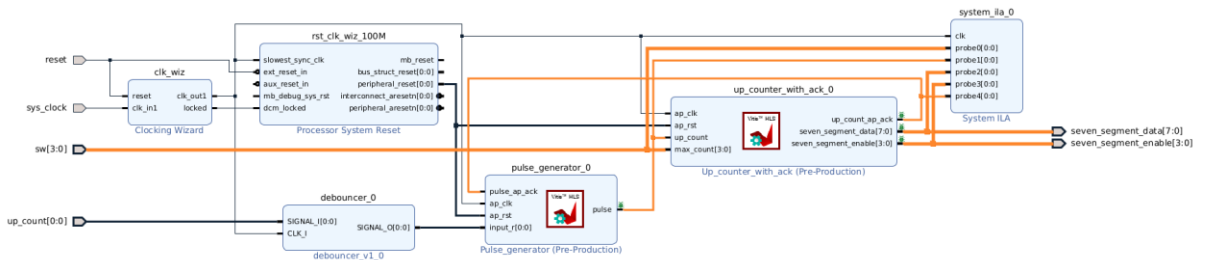


1 High-Level Synthesis for FPGA, Part 3: Advanced

- 1- Hold the control key, then, using the mouse, select desired signals.
- 2- Right-click on one of the selected signals and choose the Debug option from the drop-down menu.

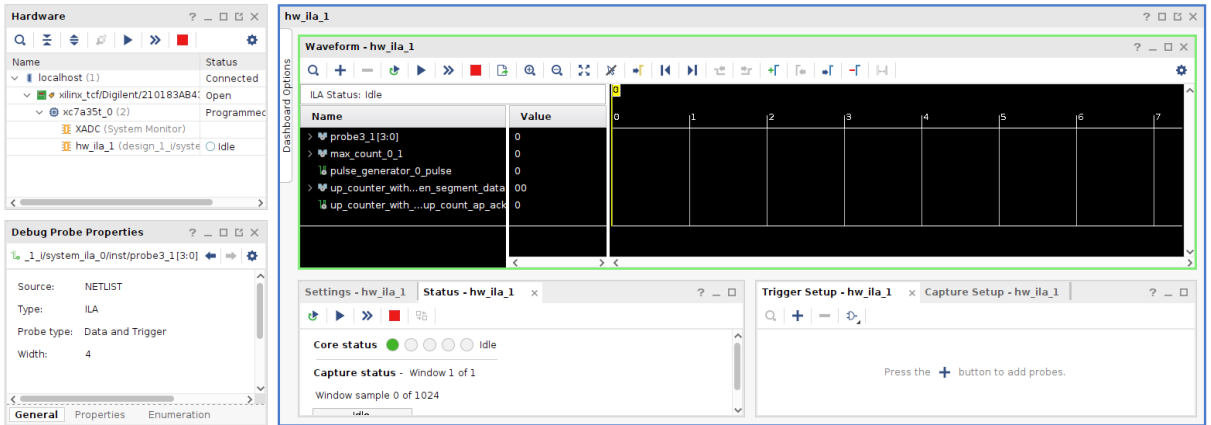


- 3- Click on the “Run Connection Automation” link and press OK after selecting all the options on the left. The debugging ILA IP will be added to the design automatically.

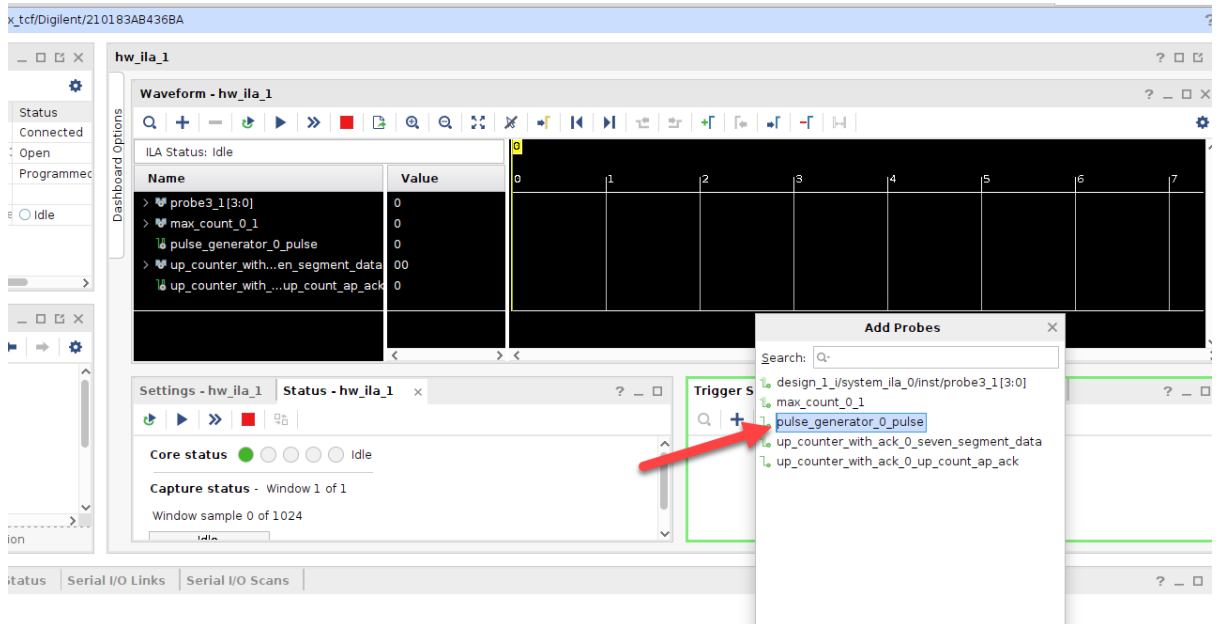


2 High-Level Synthesis for FPGA, Part 3: Advanced

- 4- Program the board. The waveform view in the debugger perspective will appear.



- 5- Click on the Add link in the Trigger setup view. And select the “pulse_generator_0_pulse” signal. Set the Value to 1.

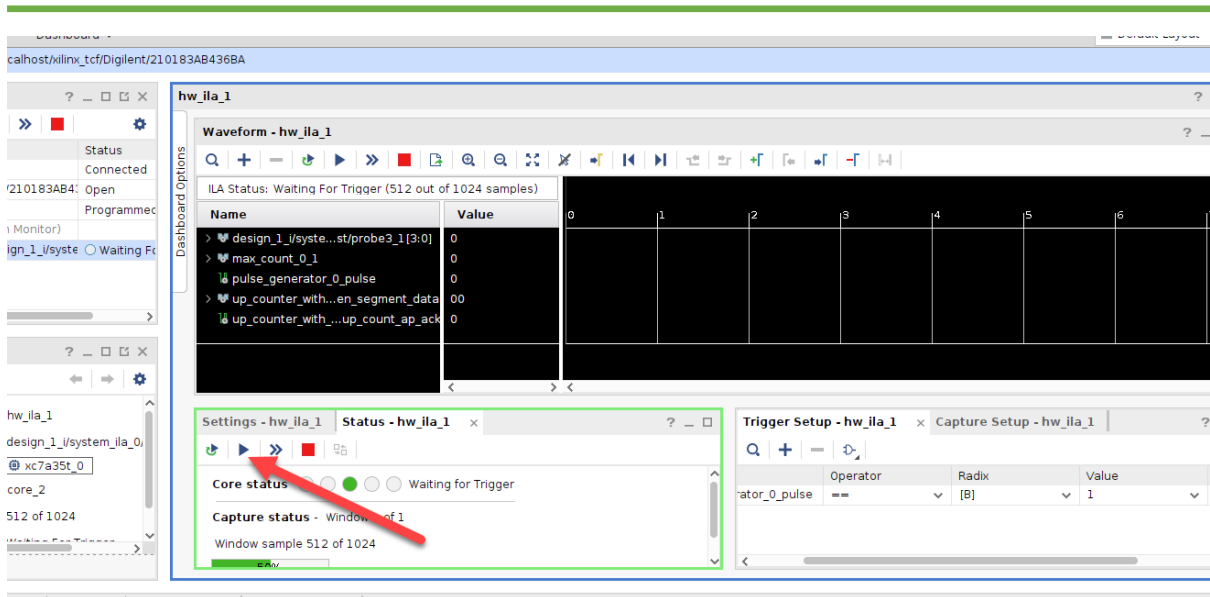


- 6- Click on the run icon in the Status view. The debugger will wait to press the UP push button on the board.

3 High-Level Synthesis for FPGA, Part 3: Advanced

Multi-Cycle Design: Example with *ack*: Quiz Solution

www.highlevel-synthesis.com



7- Press the push button and investigate the signals on the waveform viewer.

