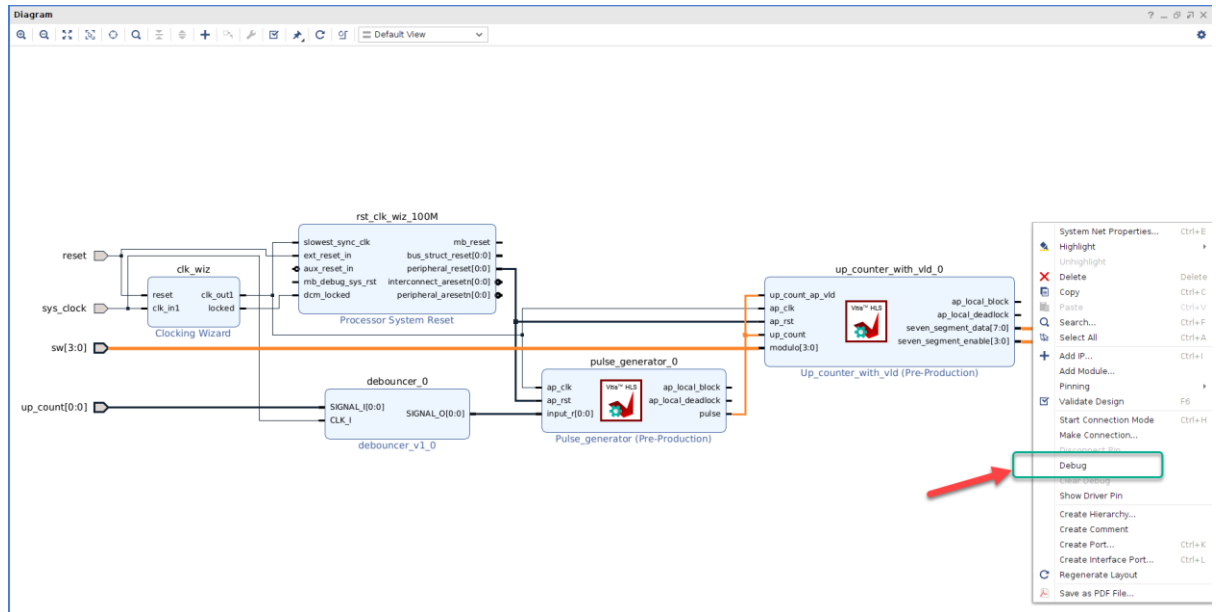


1 High-Level Synthesis for FPGA, Part 3: Advanced

- 1- Hold the control key, then, using the mouse, select desired signals.
- 2- Right-click on one of the selected signals and choose the Debug option from the drop-down menu.



- 3- Click on the “Run Connection Automation” link and press OK after selecting all the options on the left. The debugging ILA IP will be added to the design automatically.

