The in_vld signals indicate that the data on the input in signal is valid.
If the design is ready for input data, but the input valid (in_vld) is Low, the design stalls and waits for the input valid signal to be asserted to indicate a new input value is present.

The out_vld signals indicate that the data on the output out signal is valid.
When an output port is written to, its associated output valid signal is simultaneously asserted to indicate valid data is present on the port.