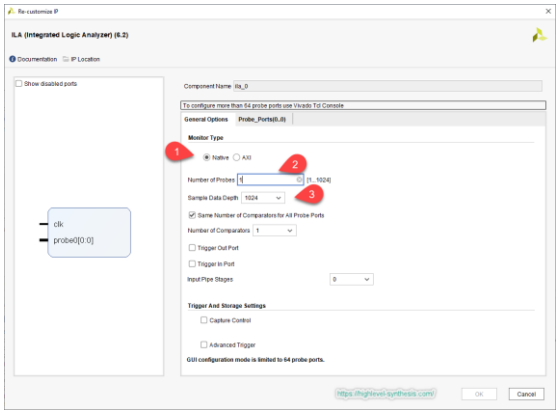
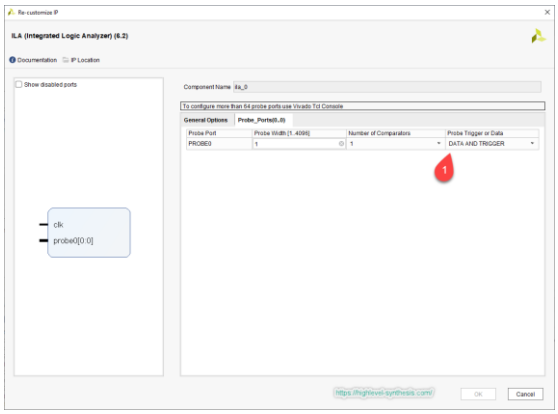
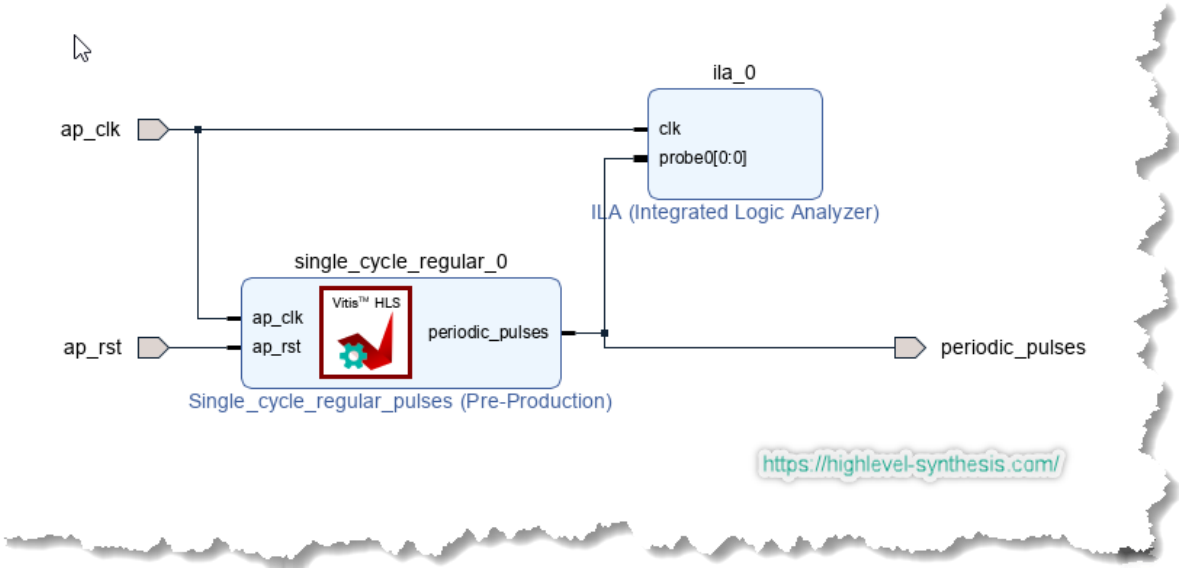
1 - Create a Vivado project and add the single_cycle_regular_pulses IP to the diagram area.

Then make the ports external. Then add an ILA IP and configure that as the following figures.





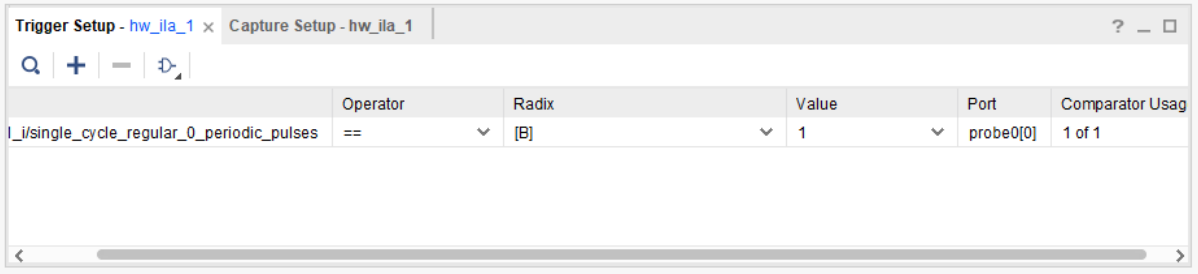
Then connect the only probe to the periodic_pulses output signal.



Add a constraint file containing these lines.

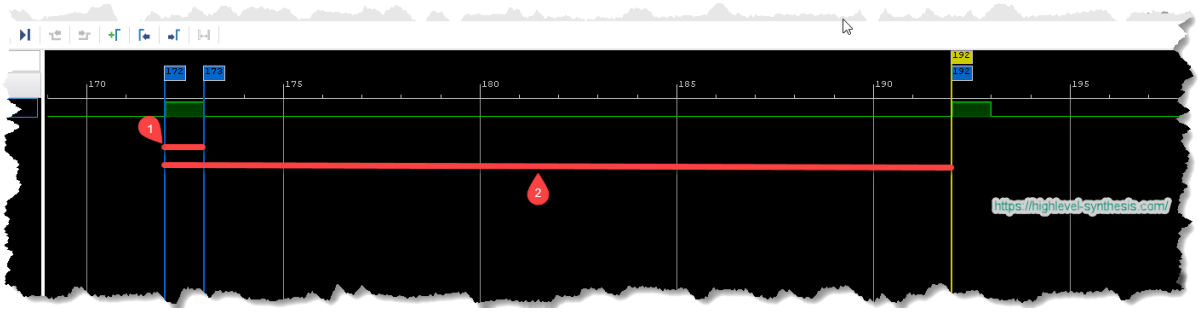
```
# Clock signal
set_property PACKAGE_PIN W5 [get_ports ap_clk]
set_property IOSTANDARD LVCMOS33 [get_ports ap_clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports ap_clk]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {periodic_pulses}]
set_property IOSTANDARD LVCMOS33 [get_ports {periodic_pulses}]

#Buttons
set_property PACKAGE_PIN U18 [get_ports ap_rst]
set_property IOSTANDARD LVCMOS33 [get_ports ap_rst]
```

Then generate the FPGA bitstream. And define the trigger Boolean expression as shown in this figure.



Now Run the ILA and check the waveform.

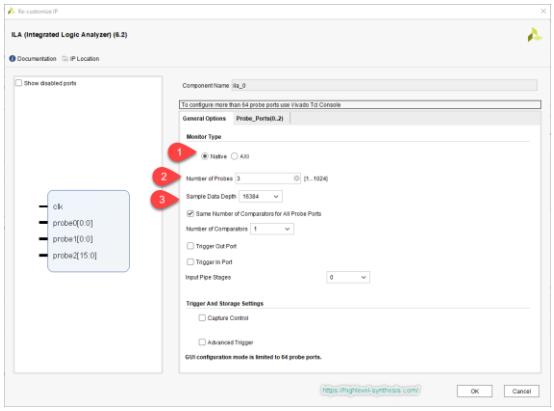
The number on the blue markers show the sample number.

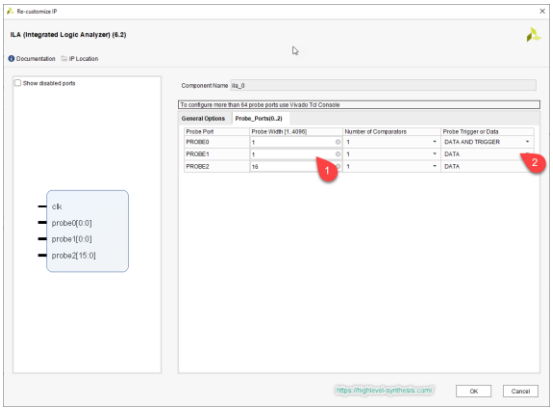


Therefore, the pulse duration is (173-172), which means one sample or one clock cycle, and the period of the regular pulse is (192-172)= 20 samples or 20 clock cycles, which is the number we have used in the HLS source file.

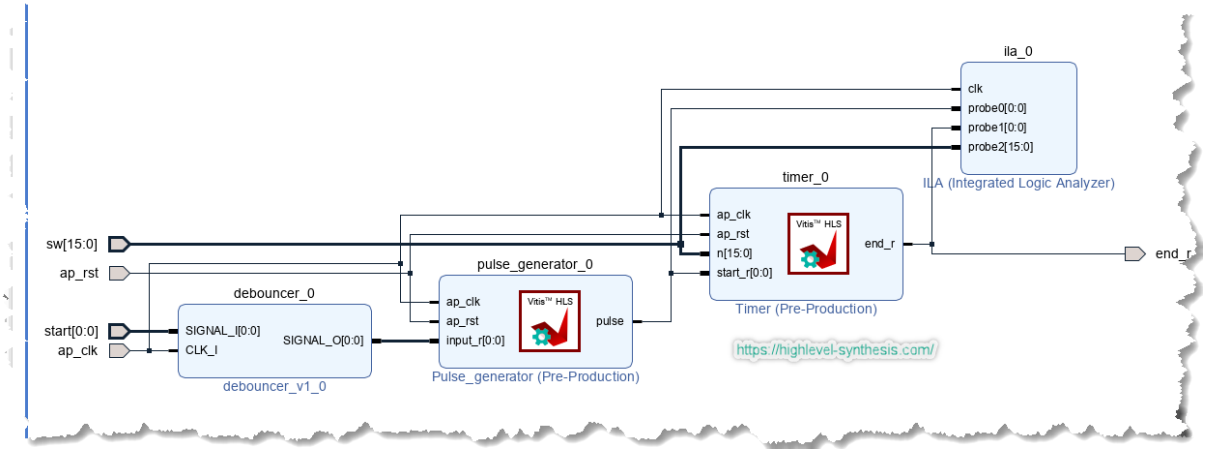
2- Create a Vivado project and add the timer IP to the diagram area.

To connect the start input to a push-button you need a debouncer and a pulse-generator IPs. Connect the IPs together and then make the ports external. Then add an ILA IP and configure that as the following figures.





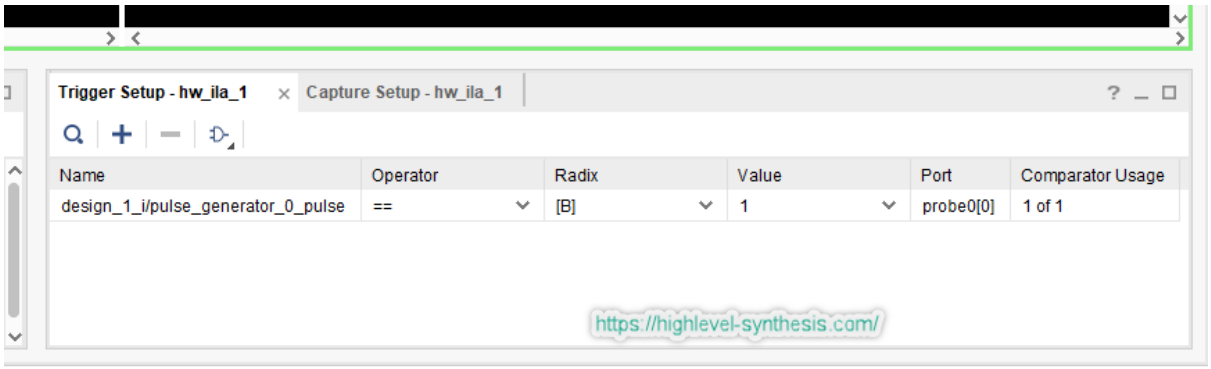
Then connect the only probe to the periodic_pulses output signal.



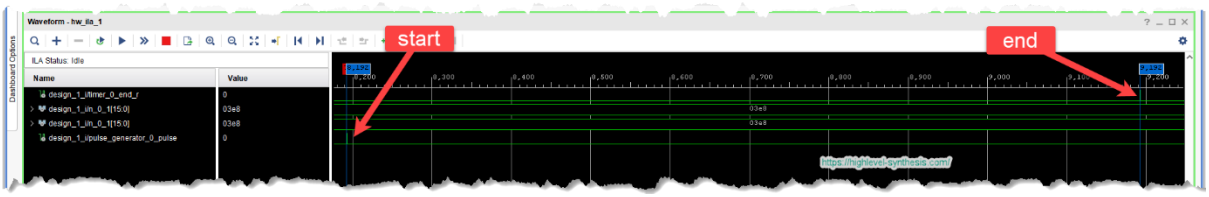
Add a constraint file containing these lines

```
# Clock signal
set_property PACKAGE_PIN W5 [get_ports ap_clk]
set_property IOSTANDARD LVCMOS33 [get_ports ap_clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports ap_clk]
# Switches
set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
set_property PACKAGE_PIN W15 [get_ports {sw[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[4]}]
set_property PACKAGE_PIN V15 [get_ports {sw[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[5]}]
set_property PACKAGE_PIN W14 [get_ports {sw[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[6]}]
set_property PACKAGE_PIN W13 [get_ports {sw[7]}]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {end_r}]
set_property IOSTANDARD LVCMOS33 [get_ports {end_r}]

#Buttons
set_property PACKAGE_PIN U18 [get_ports ap_rst]
set_property IOSTANDARD LVCMOS33 [get_ports ap_rst]
set_property PACKAGE_PIN T18 [get_ports start]
set_property IOSTANDARD LVCMOS33 [get_ports start]
```

Then generate the FPGA bitstream. And define the trigger Boolean expression as shown in this figure.



Set the number 1000 on the slide switches and then Run the ILA and check the waveform.



The distance between end and start pulses shows 1000 clock cycle or $10ms$.