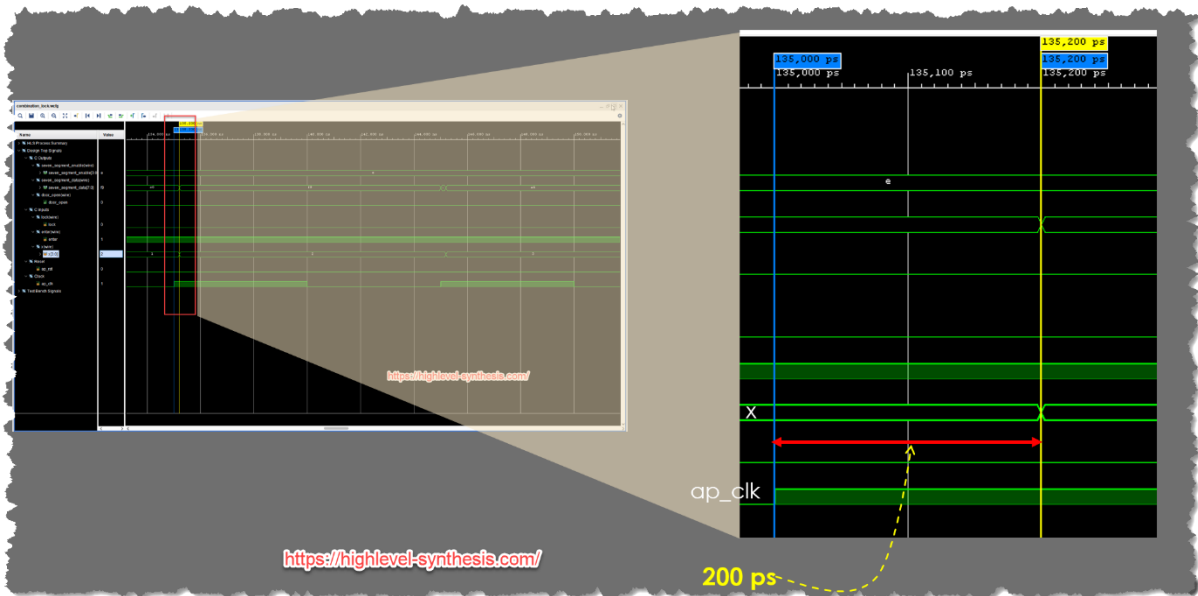


1 High-Level Synthesis in FPGA, Pat 2 – Sequential Circuits

If you look at the waveforms, there is a 200ps delay between the clock's rising edge and the new data on the x input, as shown in the following figure.

This very small delay causes the glitches that you seen in the waveforms.



In the ideal case, this delay should be zero.

It seems the simulation engine behind the scene causes this.

It is not clear to me the reason for that yet. I have contacted the Xilinx engineers, but still, I am waiting for a clear explanation.

If you find the reason, please share that with the class.