

This figure shows the C-simulation output. As can be seen, each function call generates a new data bit on the output.

```
1 INFO: [SIM 2] ***** CSIM start *****
2 INFO: [SIM 4] CSIM will launch GCC as the compiler.
3   Compiling ../../../../parallel2serial-tb.cpp in debug mode
4   Compiling ../../../../parallel2serial.cpp in debug mode
5   Generating csim.exe
6 d = 1 serial_start = 1 serial_end = 0
7 d = 1 serial_start = 0 serial_end = 0
8 d = 0 serial_start = 0 serial_end = 0
9 d = 0 serial_start = 0 serial_end = 0
10 d = 1 serial_start = 0 serial_end = 0
11 d = 0 serial_start = 0 serial_end = 0
12 d = 1 serial_start = 0 serial_end = 0
13 d = 1 serial_start = 0 serial_end = 1
14 Test Passed
15 INFO: [SIM 1] CSim done with 0 errors.
16 INFO: [SIM 3] ***** CSIM finish *****
17
```

<https://highlevel-synthesis.com/>

The following figure shows the RTL/C Cosimulation output.

