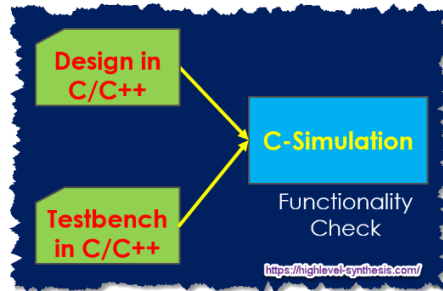
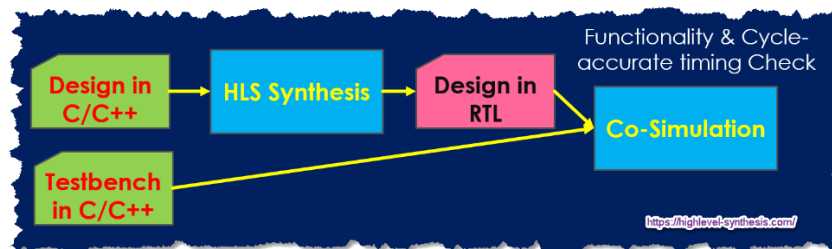


C-simulation: The C-simulation is used for checking the syntax, semantic and functional errors. It receives the C/C++ description of the design along with a testbench to apply some input data.



The C-simulation is also known as *pre-synthesis* verification. Generally, the C-simulation cannot validate the design timing and only check the functionality.

Co-simulation: The co-simulation is used for checking the RTL design functional errors and cycle-accurate timing analysis. It receives the design in RTL along with a testbench in C/C++.



The RTL/C Co-simulation is also known as *post-synthesis* verification. This step has the ability to validate the design cycle-accurate timing correctness.