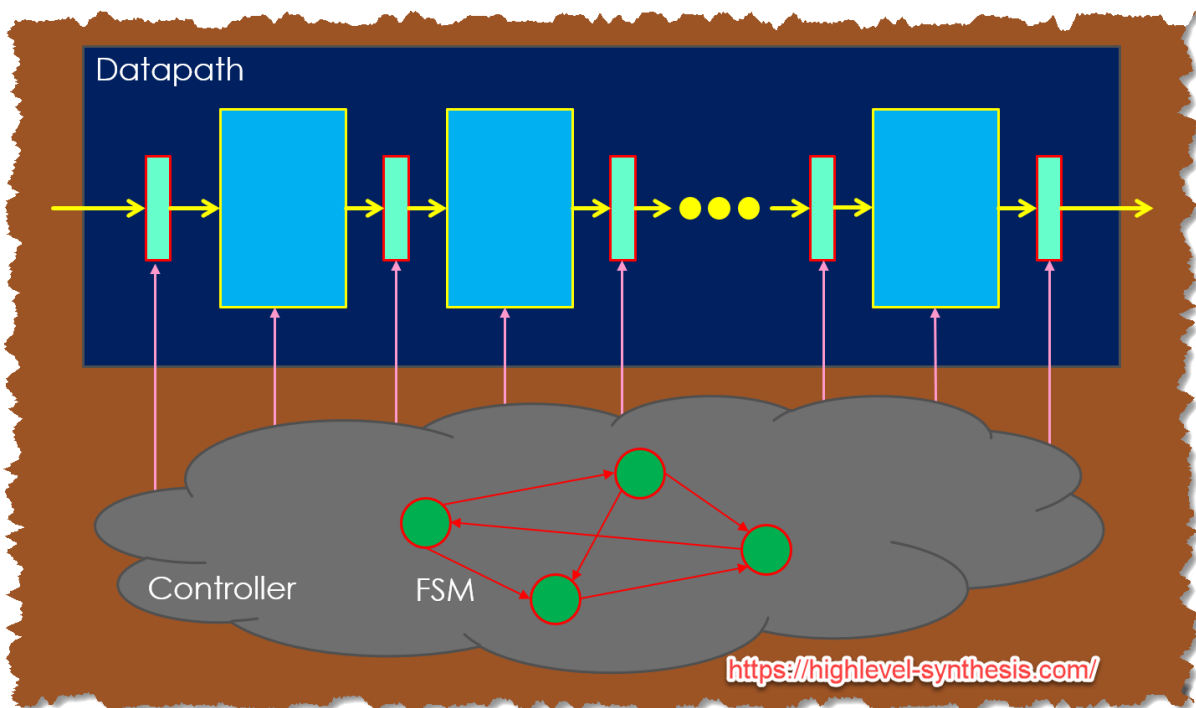


# 1 Digital System Design with High-Level Synthesis for FPGA

## Sequential Circuits

The RTL description generated by the HLS tool consists of two parts: *datapath* and *controller*. The datapath usually implements the arithmetic, data transmission and logical part of the tasks. In contrast, the controller determines the sequence of datapath tasks execution. The datapath consists of computational and logical modules connected through registers. The controller is implemented by FSMs, which contains registers to save the circuit flow states. Note that this FSM may be different from the FSM that we describe manually in the HLS code.



Control registers usually refer to the registers in the controller parts.

Moreover, state registers in VitisHLS refer to registers in the controller as well as those defined by users via static or global variables.