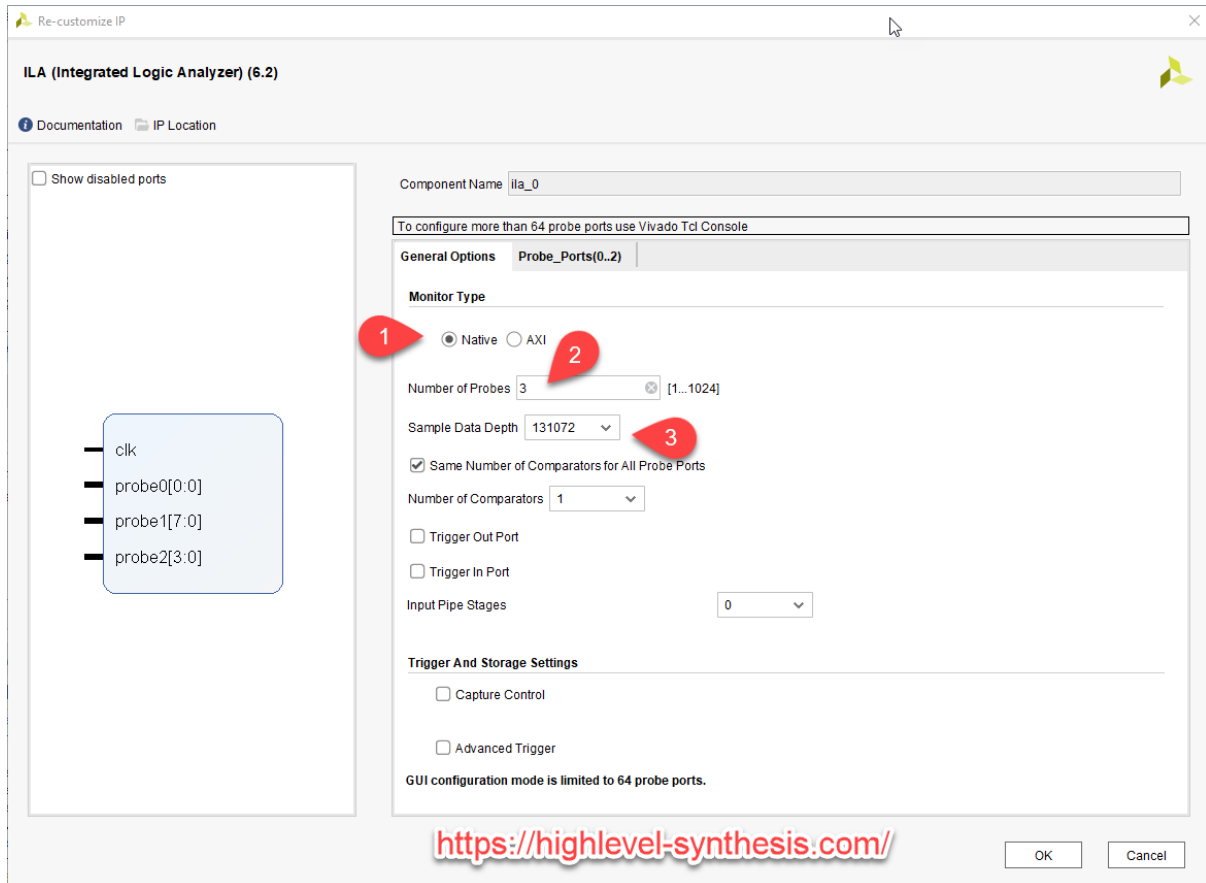


# 1 High-Level Synthesis in FPGA, Pat 2 – Sequential Circuits

7Segment-Vivado: Quiz Solution

www.highlevel-synthesis.com

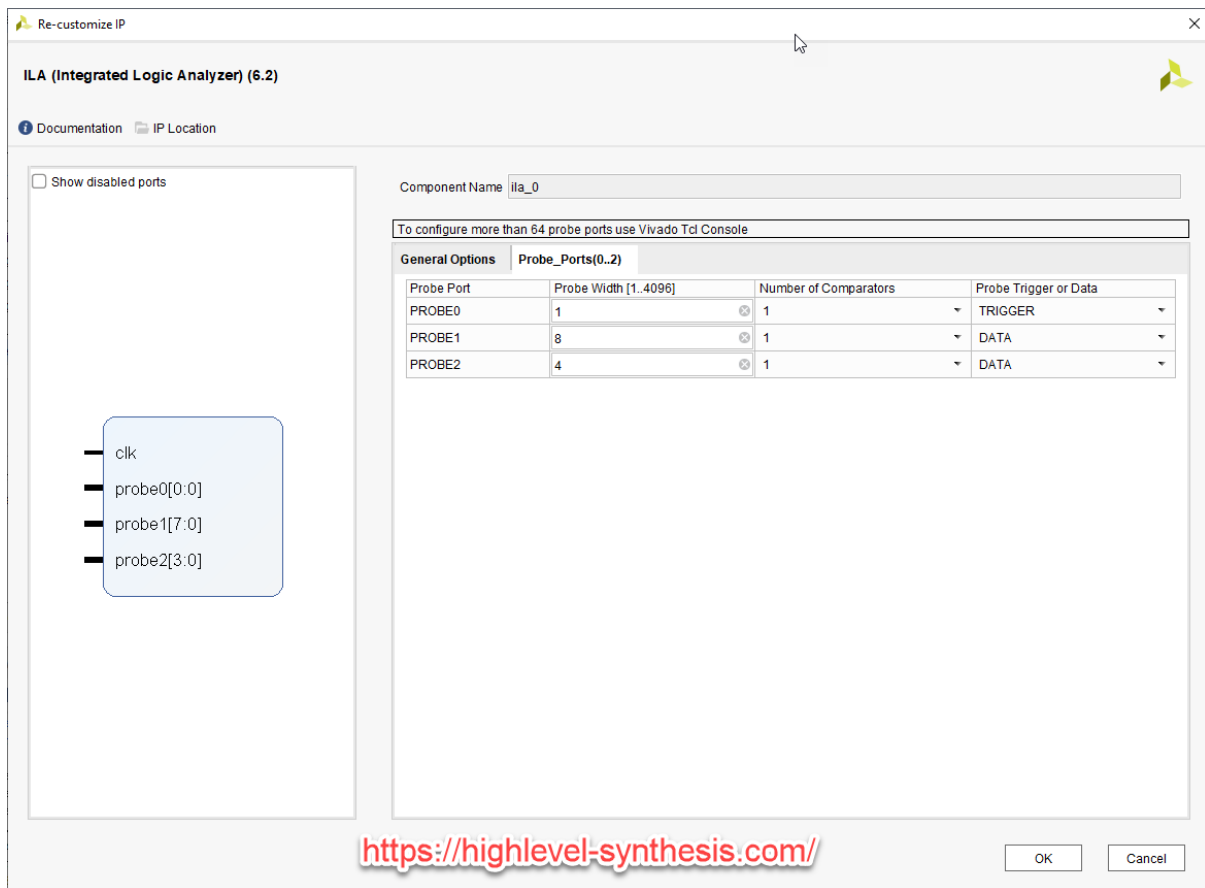
Add an ILA IP to the design and customise that as follows.



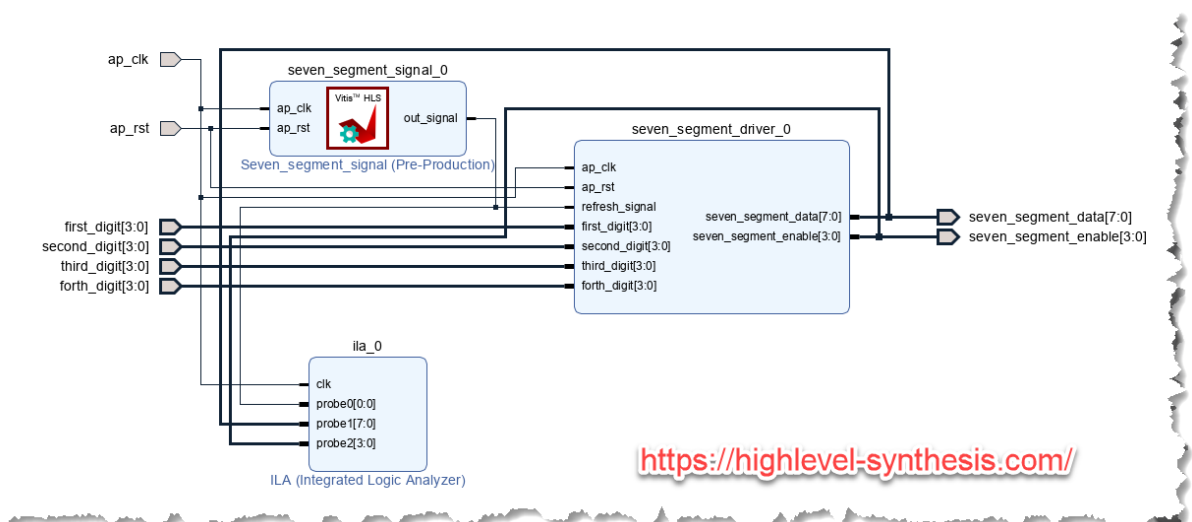
## 2 High-Level Synthesis in FPGA, Pat 2 – Sequential Circuits

7Segment-Vivado: Quiz Solution

www.highlevel-synthesis.com

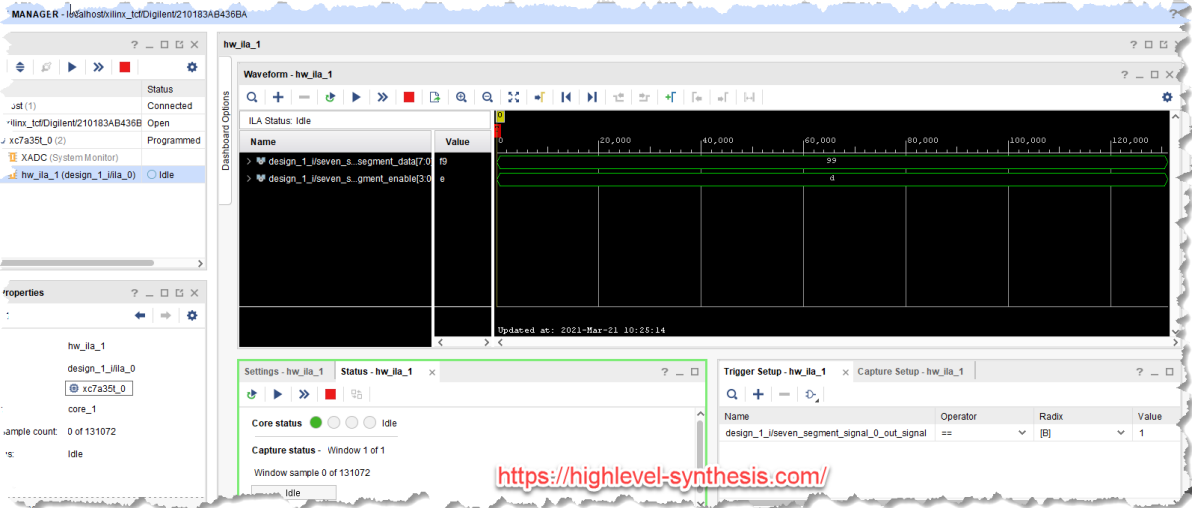


Then make the connections.



### 3 High-Level Synthesis in FPGA, Pat 2 – Sequential Circuits

Finally, this would be the output.



Please note that because there should be about 400000 samples between each to pulses of the 7-segment refresh signal, the ILA cannot show the full 7-segment refresh signal and 7-segment values in the waveform viewer. So, each time you run the runtime debugger, you will randomly see the signals for one 7-segment.