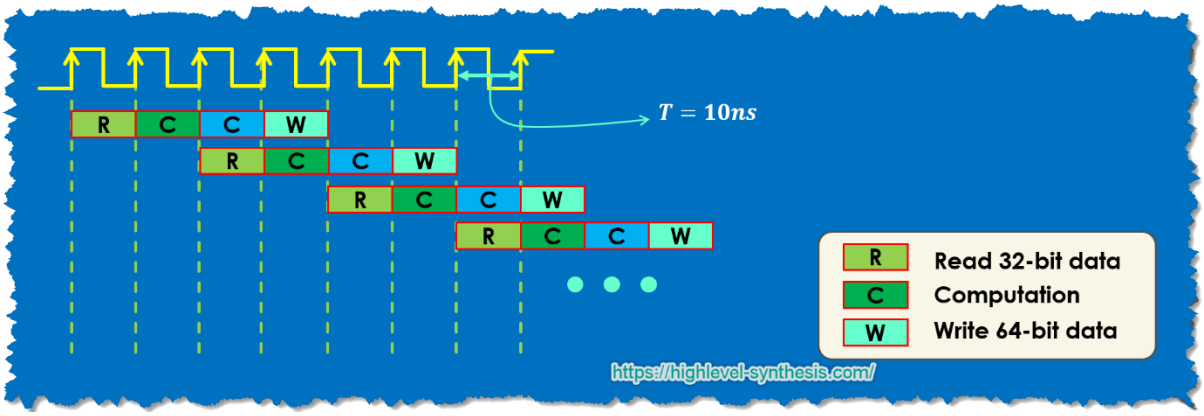

As the design accepts inputs every two clock cycles, then $II = 2$.

Latency is four ($l = 4$), as each iteration takes four clock cycle to finish.

The throughout is $\frac{64\ bit}{2*10ns} = 3.2\ Gbit/s\ or\ 400\ MByte/s$