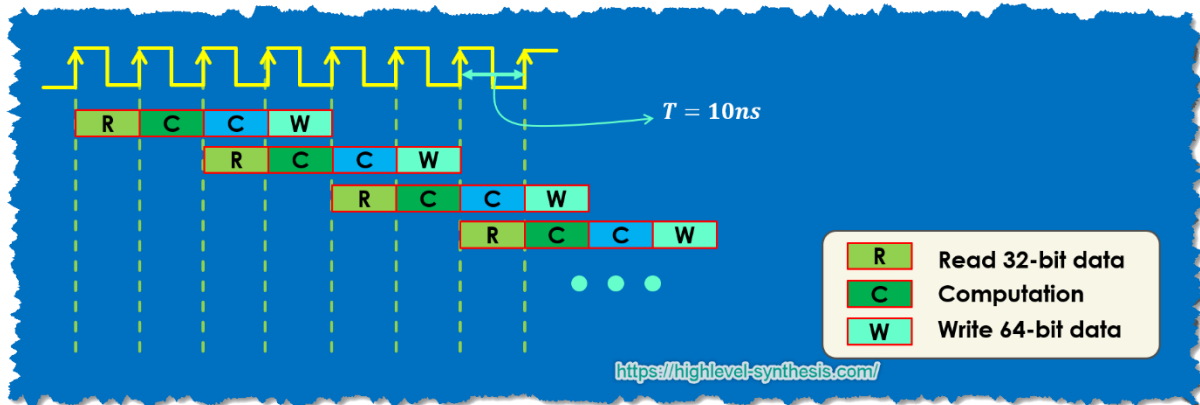


1 Digital System Design with High-Level Synthesis for FPGA

Sequential Circuits

Function-Pipelining: Performance Metric: Quiz Solution

www.highlevel-synthesis.com



As the design accepts inputs every two clock cycles, then $II = 2$.

Latency is four ($l = 4$), as each iteration takes four clock cycle to finish.

The throughput is $\frac{64 \text{ bit}}{2 * 10ns} = 3.2 \text{ Gbit/s or } 400 \text{ MByte/s}$