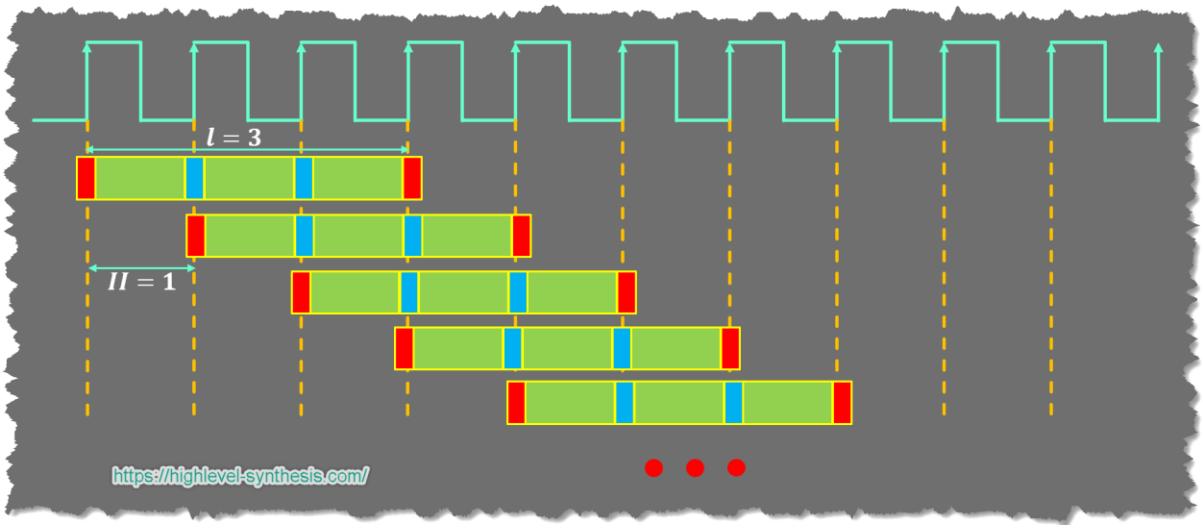
Based on the quiz assumption, the combinational circuit takes three clock cycles to generate its outputs. So, the following figure shows a possible timing diagram for the pipelined implementation.



The red registers represent the circuit state registers, and the blue ones represent the pipeline registers (registers added to the design due to the pipeline microarchitecture).