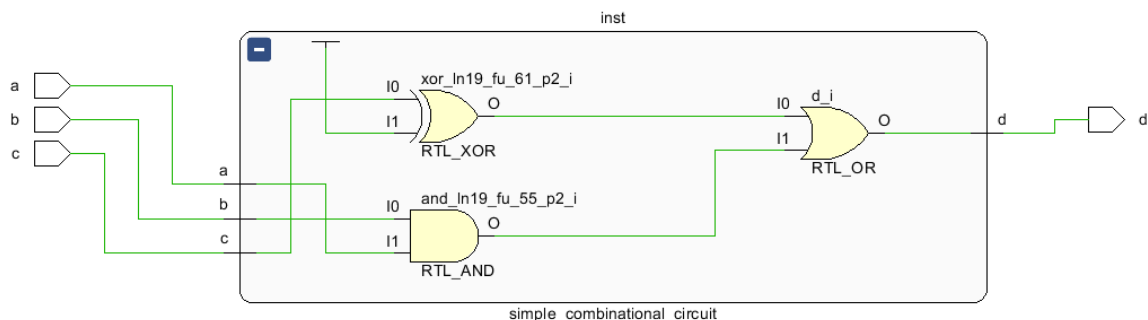


1 - “Generate Output Products ...” is one of the tasks in the IP centric design flow in Vivado Design Suite. This design flow is equipped with an extensible IP catalog Xilinx-delivered *Plug-and-Play* IP. The IPs generated by Vivado-HLS also can be used in this environment.

The IP integrator lets us create complex designs by instantiating and interconnecting IPs in the diagram window. These IPs are customisable, and their parameters can be modified by designers or automatically by other connected IPs. To customise an IP just double-click on the IP instance in the design canvas and change the provided parameters in the opened window. Note that not all IPs have parameters for customisation.

After connecting and customising the IPs in our design, we should run the “Generate Output products...” tasks. This task generates few files (such as XCI and DCP) for the IPs and a behavioural simulation model and creates an elaborated design.

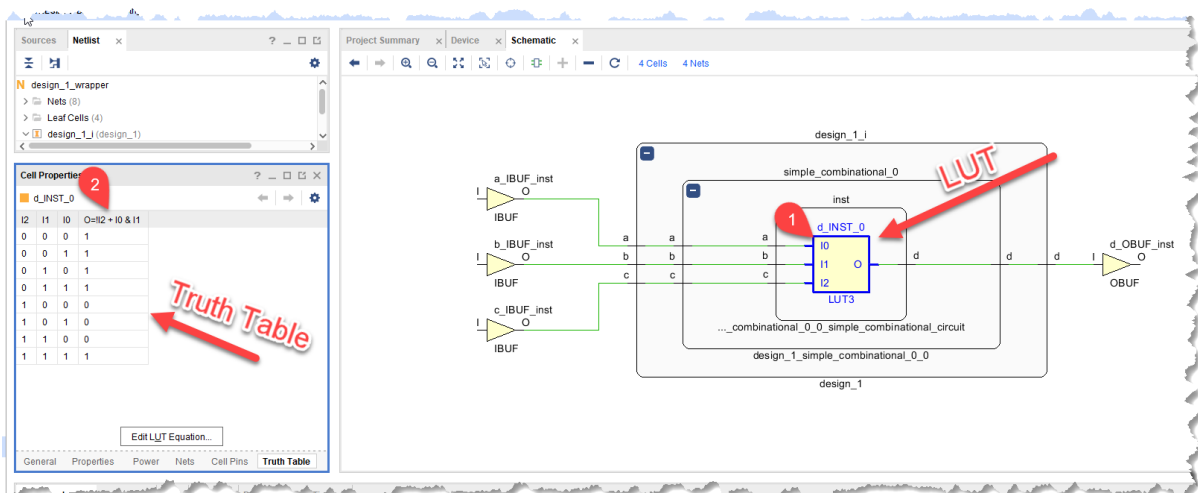
For example, let’s consider the *simple_combinational_circuit* example presented in Section 6- Lecture 42 and 43. Now if you click on “RTL ANALYSIS→open elaborated design→Schematic” in the “Flow Navigator” view immediately after generating the output products then you will see the following schematic for the design which is not mapped to the FPGA yet.



The XCI file is an IP-XACT component instance XML file that records the values of project options, customisation parameters, and port parameters used to create the IP. Most of the IP in the Vivado IP catalog uses the IP-XACT standard format (based on IEEE Std 1685-2009) [UG895].

A design checkpoint (DCP) is a file used by the Vivado Design Suite that represents a snapshot of a design at any stage of the design process. The snapshot includes the netlist, constraints and implementation results [Design Checkpoints]. Xilinx recommends that you generate the DCP file to reduce synthesis time for the top-level design [UG939].

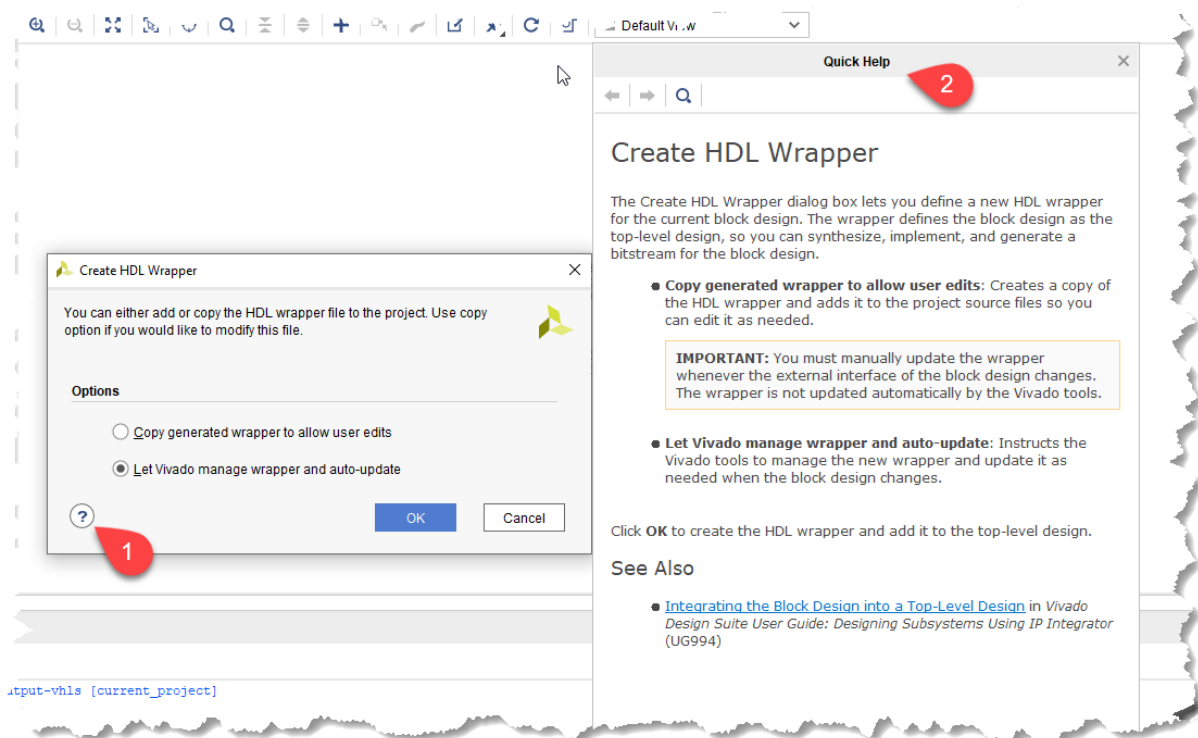
For your information: if you open the elaborated design after performing synthesis and implementation, you will see the following schematics that implements the simple_combinational_circuit example. Also, you can see the truth table in the Cell Properties view, as shown in the following figure.



2- Create HDL Wrapper

This option creates a top-level HDL file and adds it to the source list. The top-level HDL wrapper around the block design is needed because a BD source cannot be synthesised directly [UG994].

You get more information by clicking on the quick help icon in the Create HDL Wrapper.



Also, you can see the generated Verilog or VHDL file.

4 Digital System Design with High-Level Synthesis in FPGA

Vivado Generate Output Products and Design Wrapper

www.highlevel-synthesis.com

