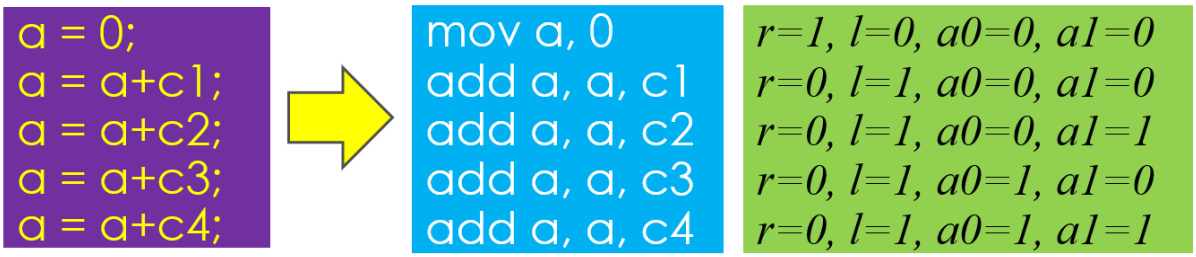
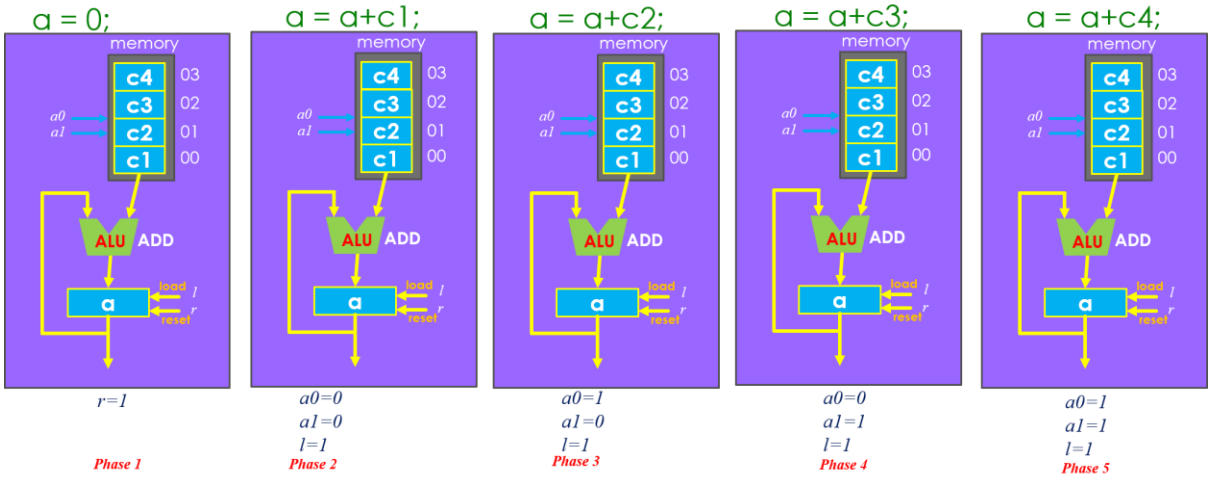
According to the CPU architecture, the original C code can be translated to the assembly and machine code shown in the following figure.

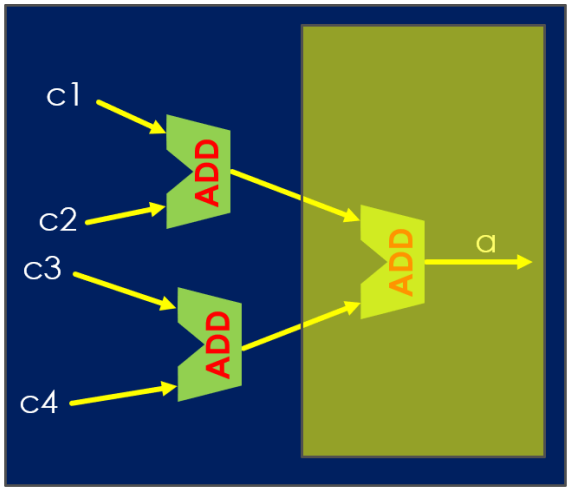


Our CPU can perform only one operation at the time as it has only one ALU, one memory bank and one register. Therefore, five steps or phases are required to execute the code.

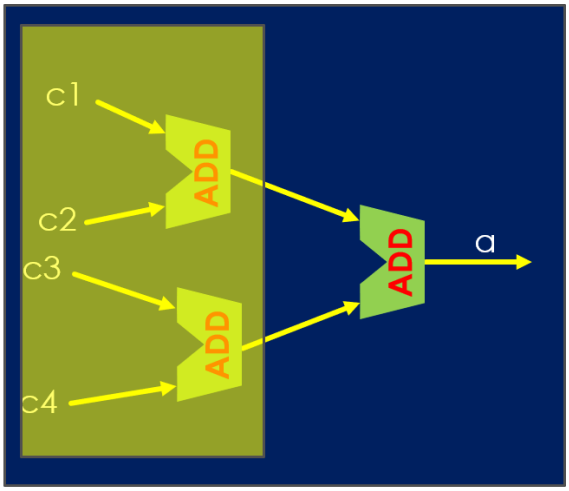


On the other hand, the dataflow graph of the FPGA implementation shows that the first two adders on the left can run together and generate their output. Then the right-hand side adder generates the output at the second phase.

Therefore, the following figure shows the two-step code execution on the FPGA.



Phase 1



Phase 2