If we consider the default design clock period, as shown in Figure 1, and synthesis the code, then Figure 2 shows the synthesis report. In addition, Figure 3 depicts the design execution schedule taken from the analysis perspective.

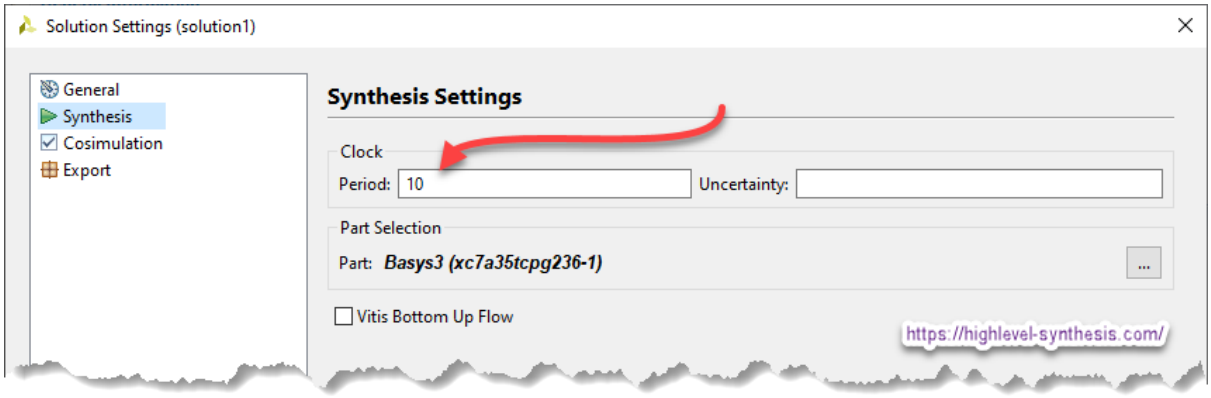


Figure 1

As can be seen, the design requires three steps to finish. Moreover, each step takes about 10ns. According to the label 2 in Figure 2, the design latency is 30ns. Therefore, if we change the design clock period from 10 to 30 (as shown in Figure 4), we should expect to have a fully combinational circuit.

The synthesis report in the last figure confirms that.

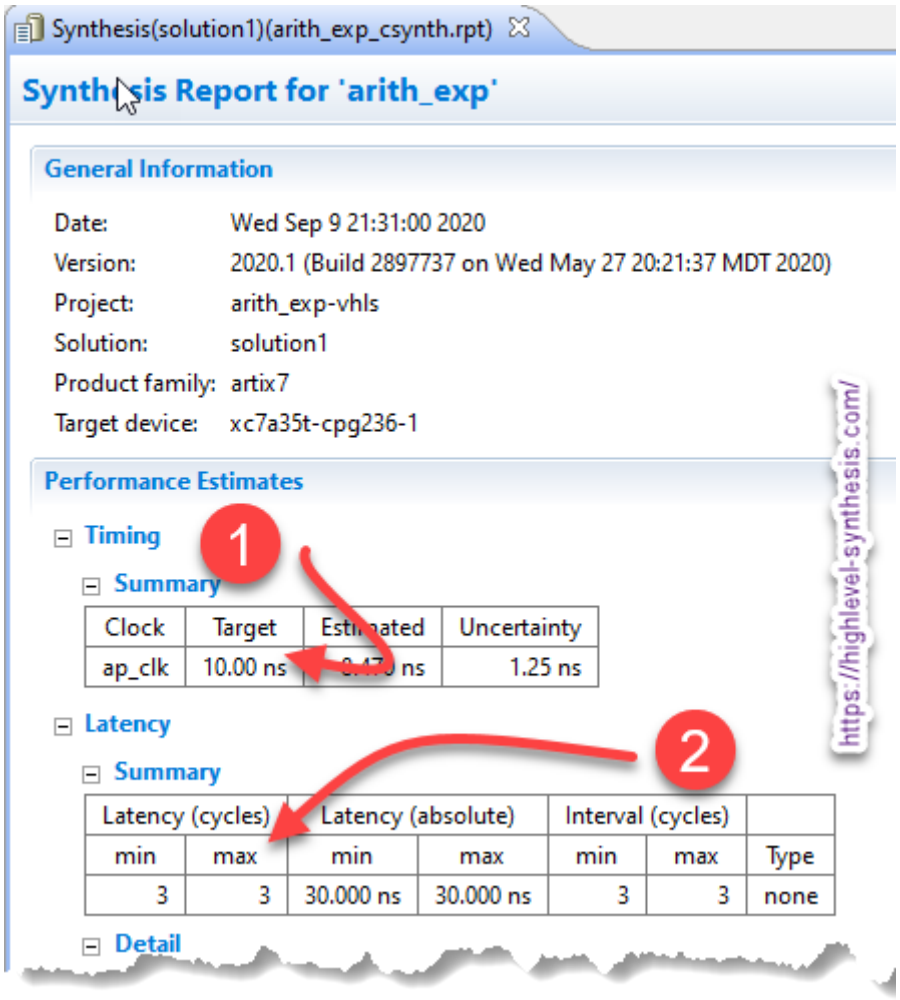


Figure 2 1) design clock period 10ns 2) design requires 3 cycles to finish

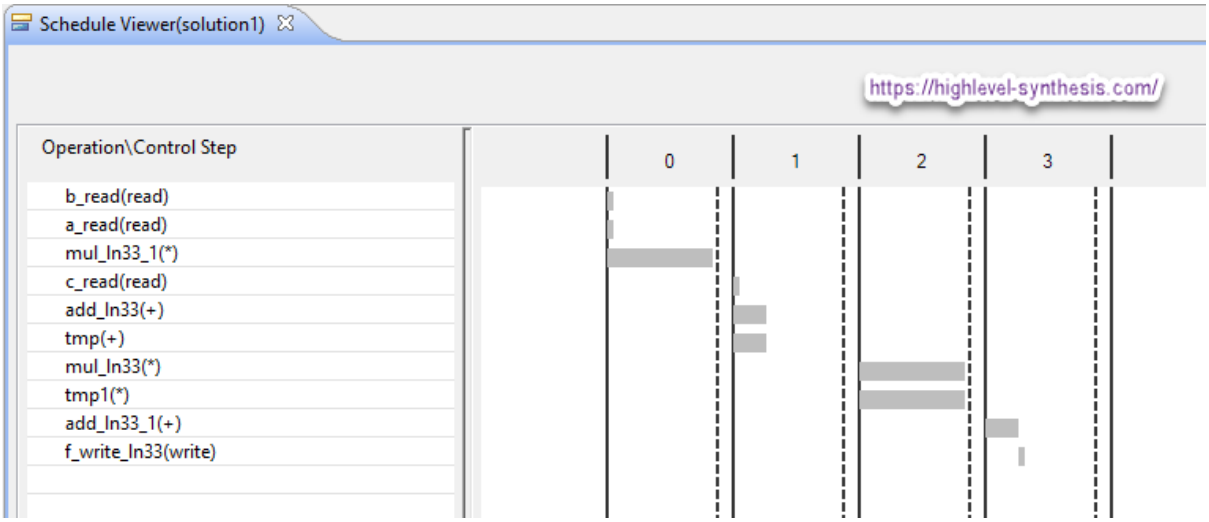


Figure 3

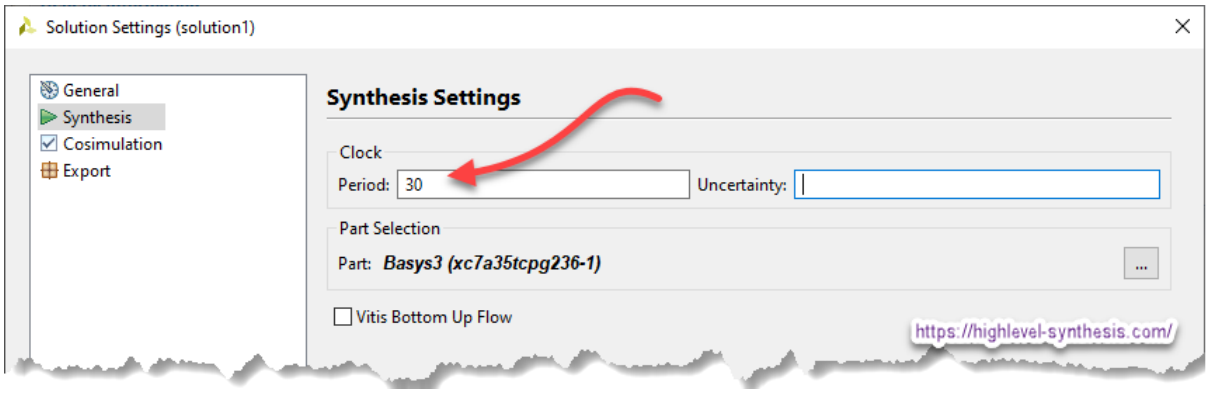
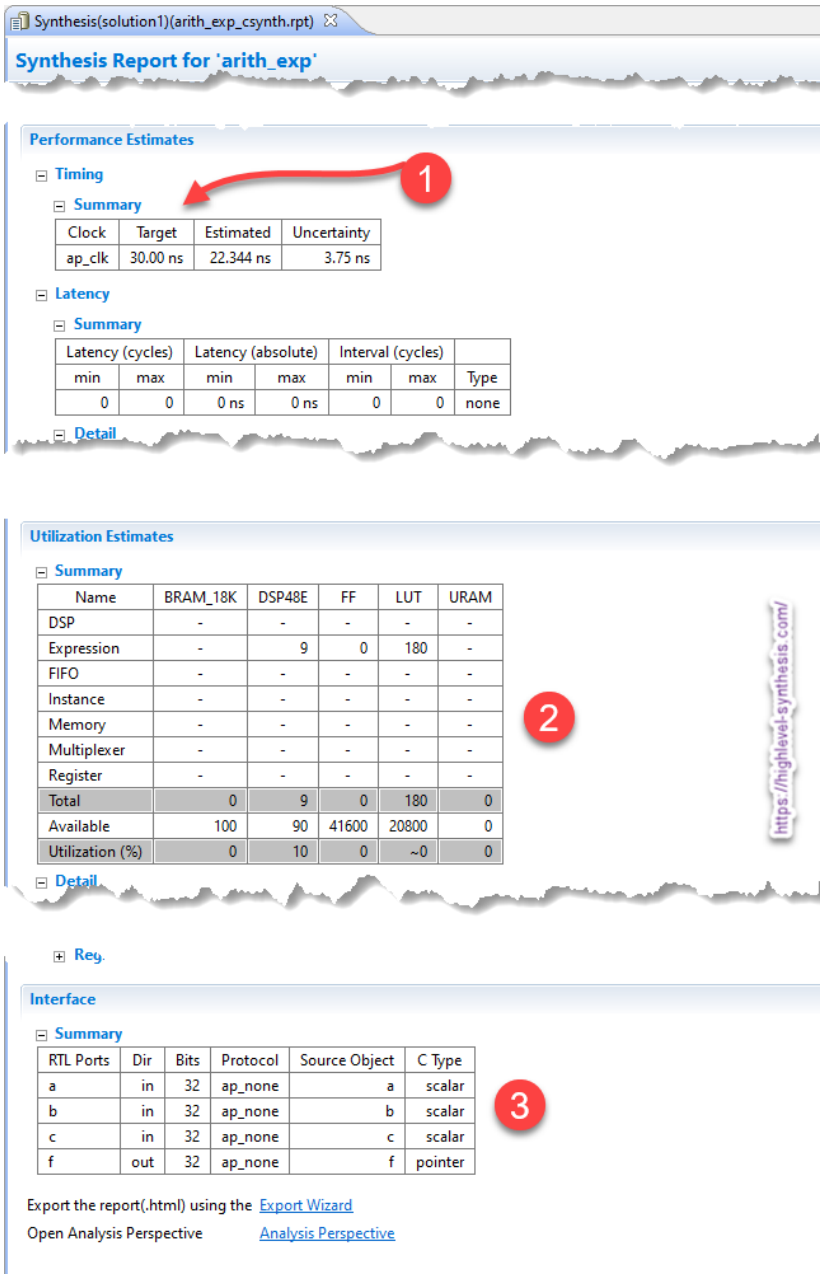

Solution Settings (solution1)
General
Synthesis
Cosimulation
Export
Synthesis Settings
Clock
Period: 30
Uncertainty:
Part Selection
Part: Basys3 (xc7a35tcpg236-1)
...
Vitis Bottom Up Flow
https://highlevel-synthesis.com/

Figure 4



Synthesis(solution1)(arith_exp_csynth.rpt)

Synthesis Report for 'arith_exp'

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	30.00 ns	22.344 ns	3.75 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
0	0	0 ns	0 ns	0	0	none

Detail

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	9	0	180	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	-	-
Register	-	-	-	-	-
Total	0	9	0	180	0
Available	100	90	41600	20800	0
Utilization (%)	0	10	0	~0	0

Detail

Reg.

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
a	in	32	ap_none	a	scalar
b	in	32	ap_none	b	scalar
c	in	32	ap_none	c	scalar
f	out	32	ap_none	f	pointer

Export the report(.html) using the Export Wizard

Open Analysis Perspective Analysis Perspective

Figure 5 1) design clock period = 30ns, 2) no memory cell 3) only top-function arguments among the ports