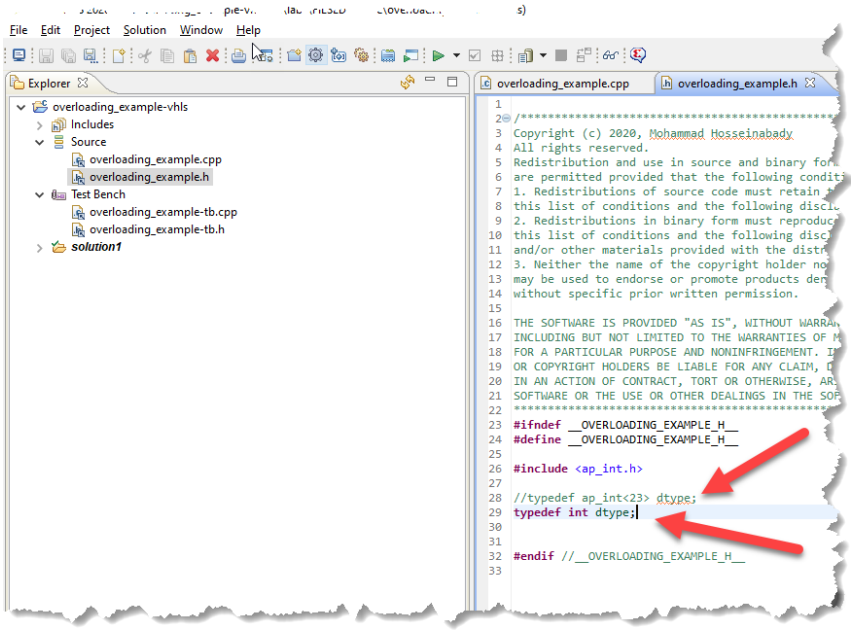
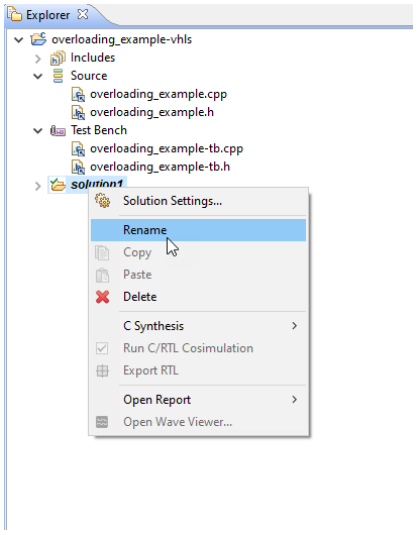
To compare the synthesis reports of two or more design configurations, we need a different solution for each of them.

Let's consider the *overloading_example* in which we want to compare the synthesis reports for two designs using two different data types.



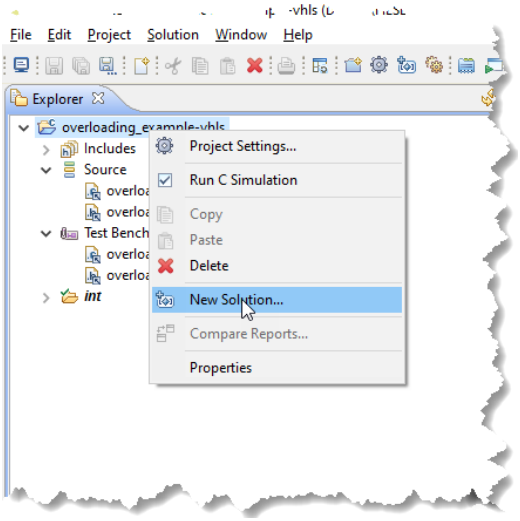
First, let's change the name of **solution1** folder with a more meaningful one, for example, "*int*". For this purpose, right-click on the folder and select the *rename* option and then change the name.



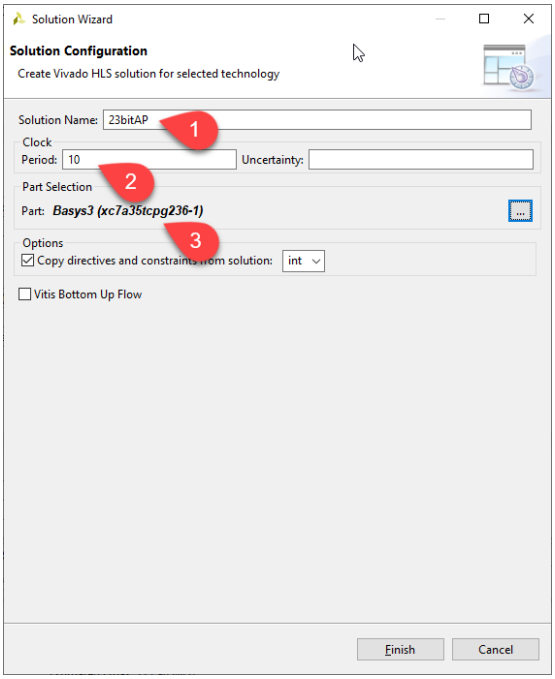
Now, synthesise the design.

Let's go to the next design configuration

First, create a new solution. For this purpose, right-click on the project name in the explorer view and select the "New Solution" option.

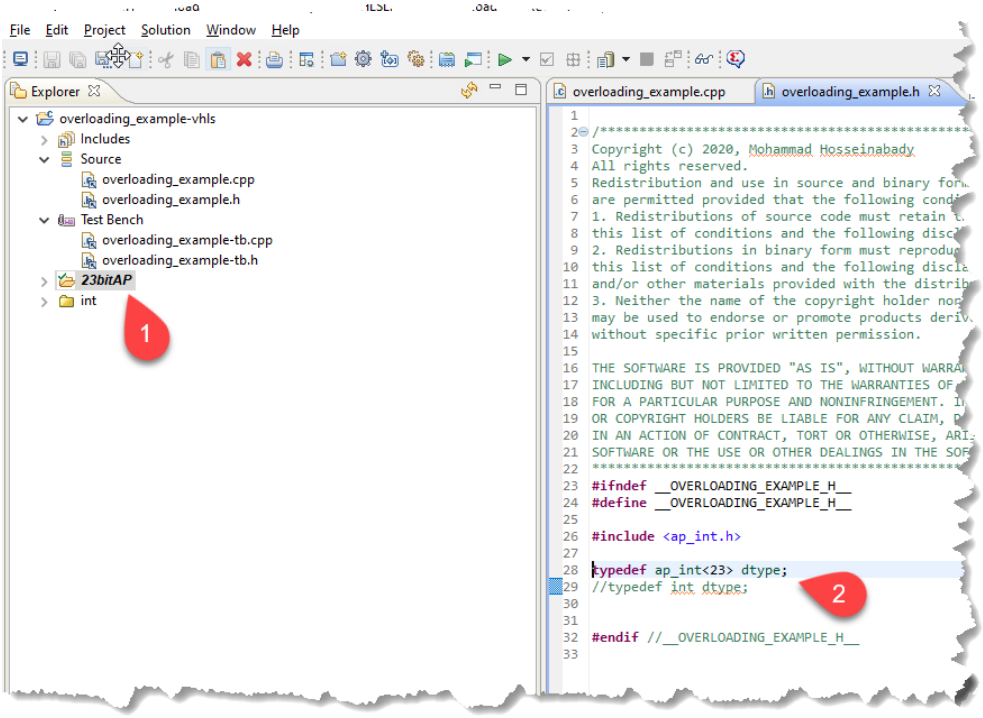


Then select a new name for the solution (for example to *23bitAP*) and change the configuration if you wish.



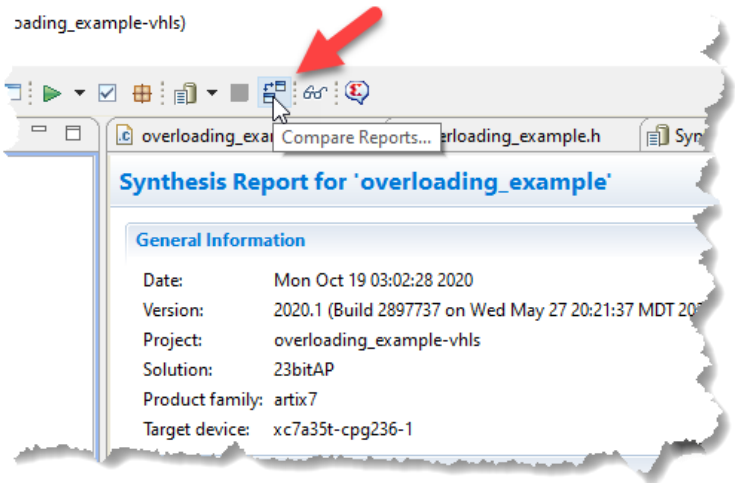
Make sure that the new solution is highlighted as the active solution in the project hierarchy. If it is not, then right-click on the solution folder as select the “Set Active Solution” option.

Then change the design (the design code or project configuration such as clock period constraint) and perform the synthesis process again.

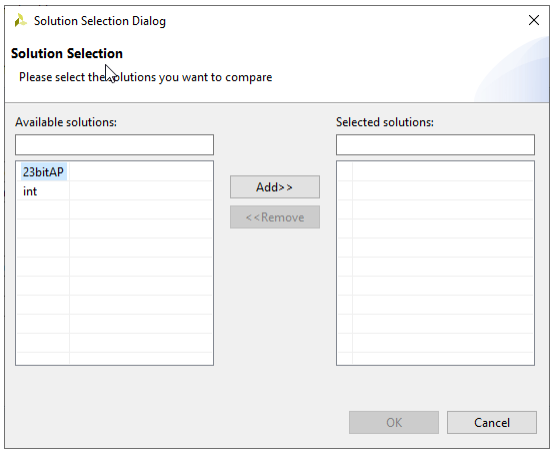


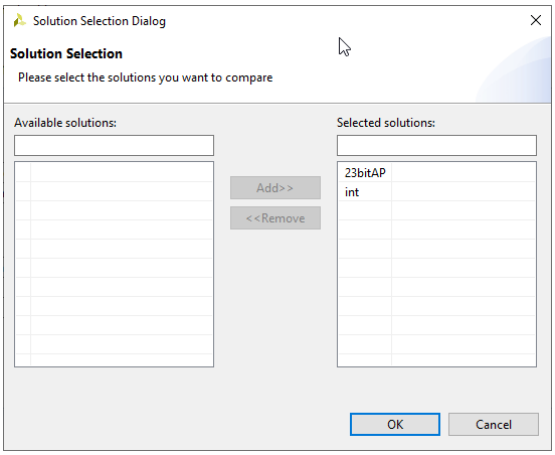
Now we are ready for the report comparison.

Click on the “Compare Reports” icon.

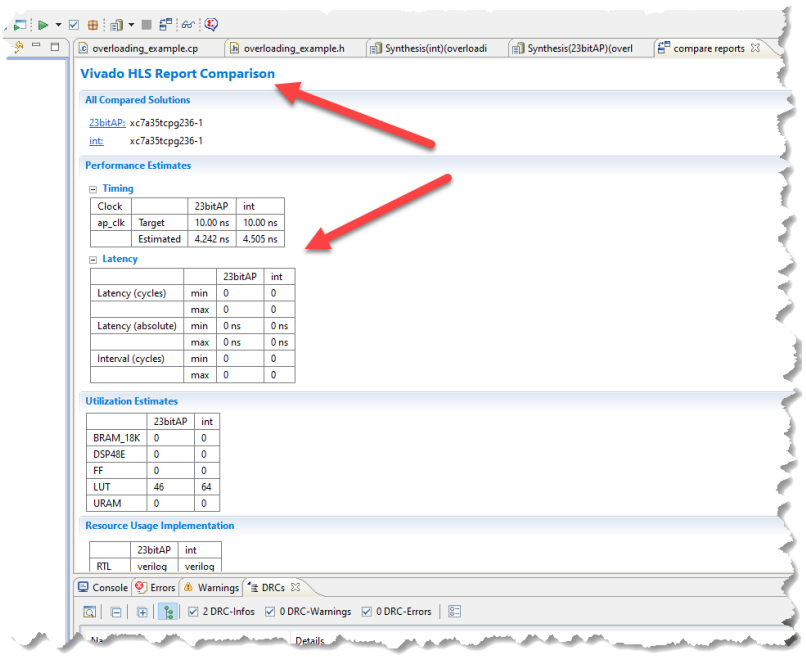


In the “Solution Selection Dialog”, add the desired solutions to the “Selected Solution” part on the right and press OK.





Then you will have the “Vivado HLS Report Comparison” window.


overloading_example.cp
overloading_example.h
Synthesis(int)(overloadi
Synthesis(23bitAP)(overl
compare reports
Vivado HLS Report Comparison
All Compared Solutions
23bitAP: xc7a35tcpg236-1
int: xc7a35tcpg236-1
Performance Estimates
Timing
Clock | | 23bitAP | int
ap_clk | Target | 10.00 ns | 10.00 ns
| Estimated | 4.242 ns | 4.505 ns
Latency
| | 23bitAP | int
Latency (cycles) | min | 0 | 0
| max | 0 | 0
Latency (absolute) | min | 0 ns | 0 ns
| max | 0 ns | 0 ns
Interval (cycles) | min | 0 | 0
| max | 0 | 0
Utilization Estimates
| 23bitAP | int
BRAM_18K | 0 | 0
DSP48E | 0 | 0
FF | 0 | 0
LUT | 46 | 64
URAM | 0 | 0
Resource Usage Implementation
| 23bitAP | int
RTL | verilog | verilog
Console
Errors
Warnings
DRCs
2 DRC-Infos
0 DRC-Warnings
0 DRC-Errors
Details